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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

A CAHNERS PUBLICATION

April 15, 1993

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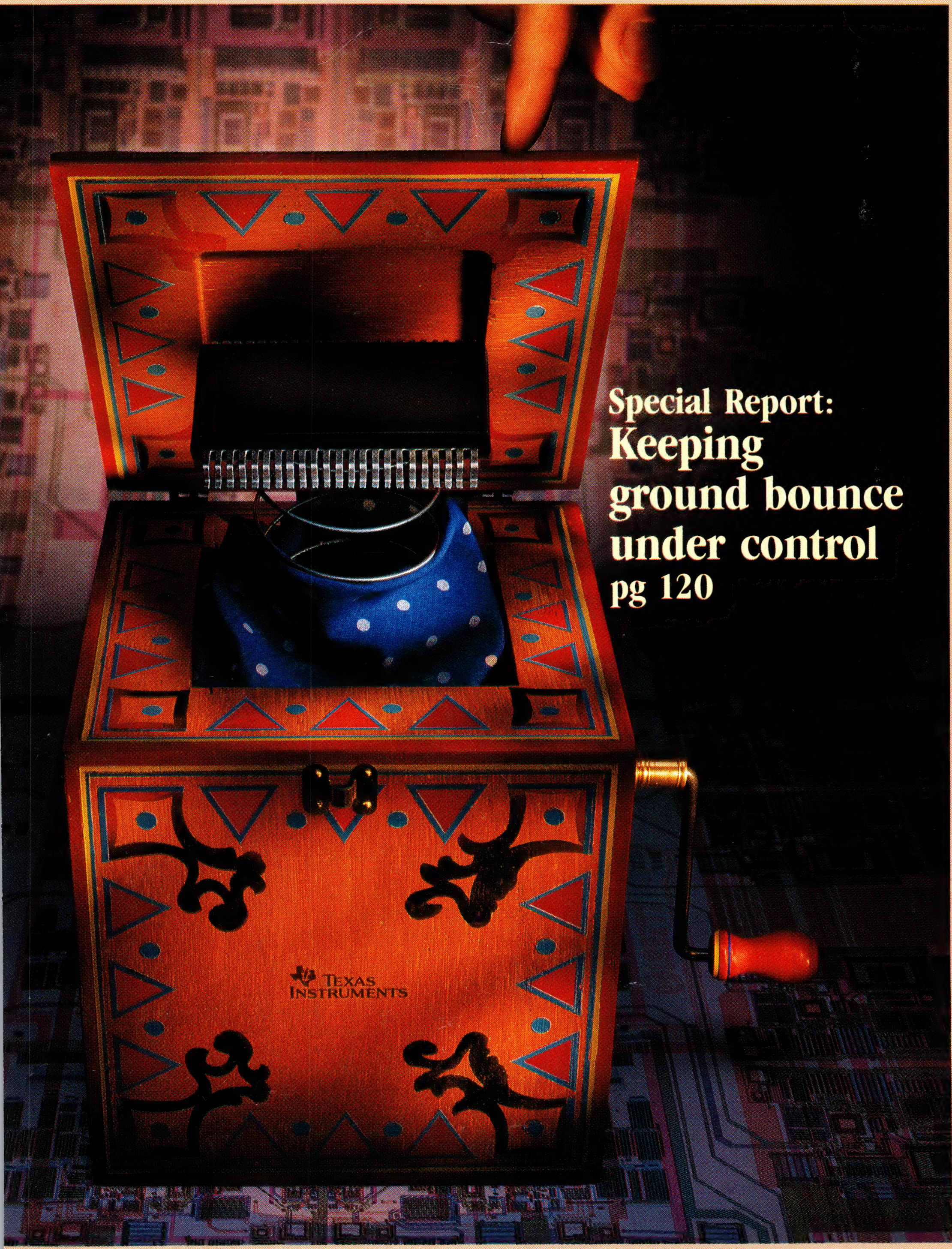

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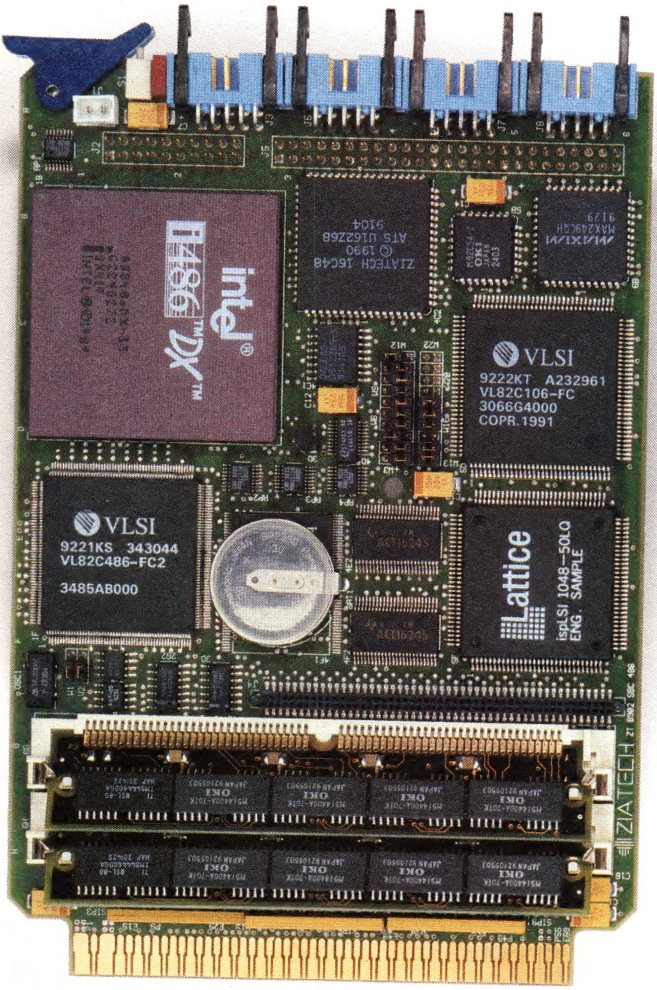
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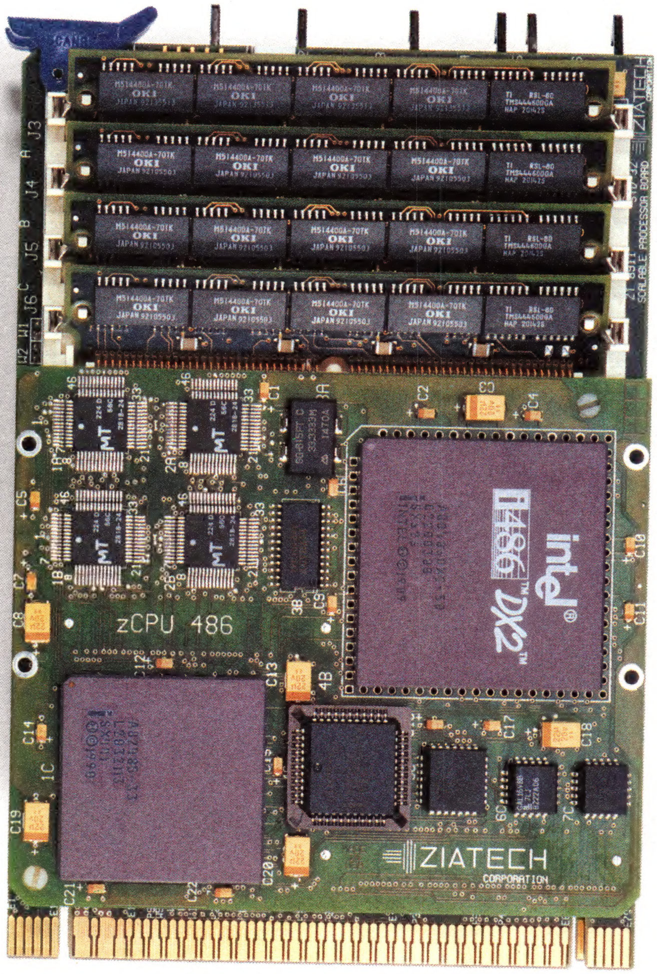

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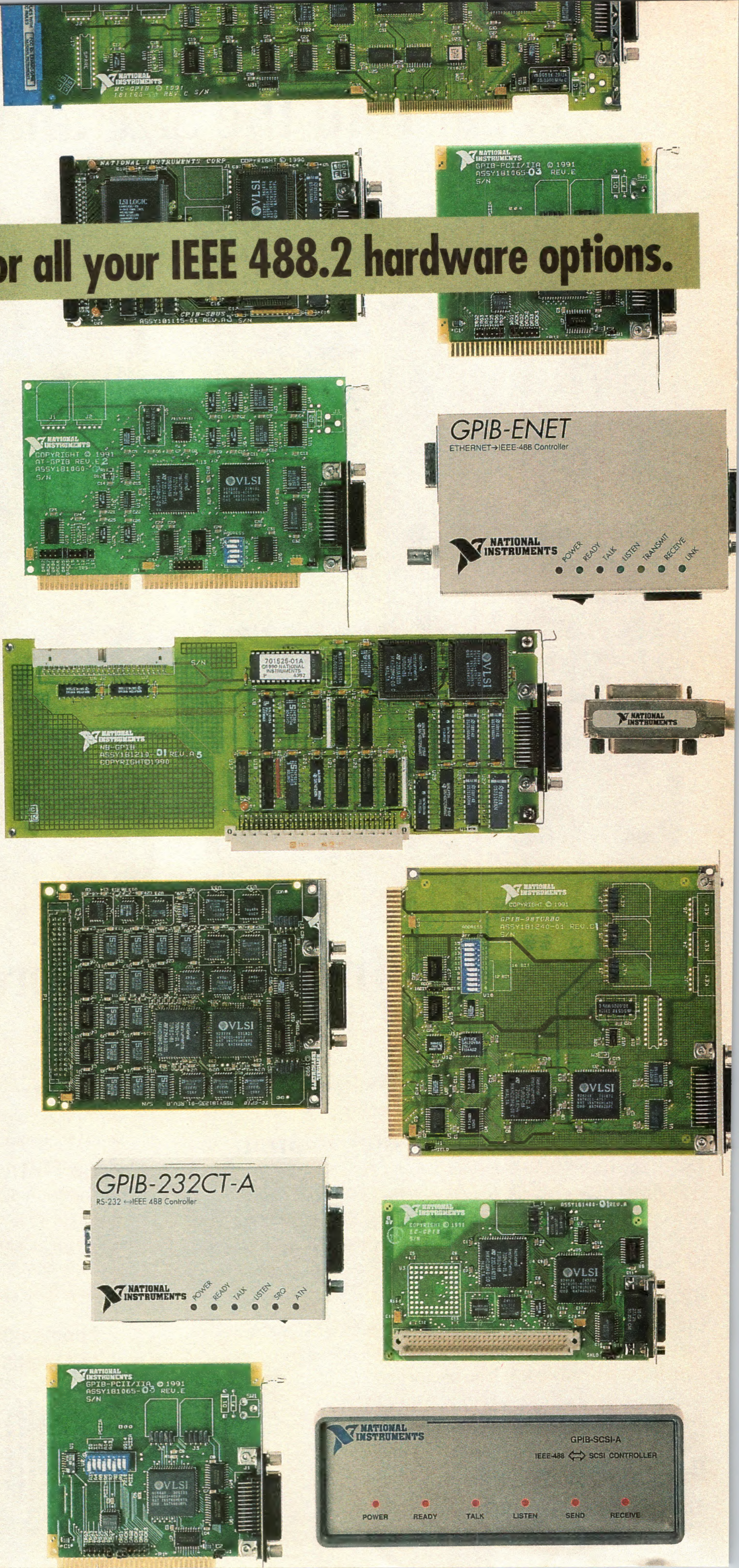

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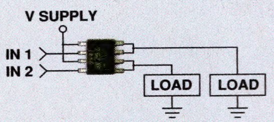

Device	Breakdown Voltage (V)	On-Resistance (Ω)	Current (A)
Si9433DY	-12	0.075 @ V_{GS}= -4.5V	±5.1
single p-ch	-12	0.110 @ V_{GS}= -2.7V	±4.0
Si9933DY	-12	0.13 @ V_{GS}= -4.5V	±3.8
dual p-ch	-12	0.21 @ V_{GS}= -2.7V	±3.0

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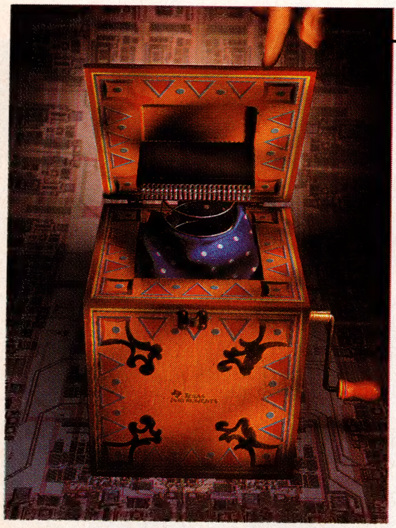

On the cover: Although ground bounce will never go away entirely, manufacturers have made strides to reduce it in their latest bus-driven ICs. In this Special Report, devices are compared under identical conditions, allowing you to use the results to choose the product you need. (Photo courtesy Texas Instruments Inc; art direction, Ken Martin; photography, Rusty Hill). . . . **PAGE 120**

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.

SPECIAL REPORT

EDN ground-bounce tests revisited

Ground bounce can cause the failure of ICs, intermittent problems in systems, and possibly even the death of a product. It is critical that you evaluate your design to see if ground bounce will affect it. These tests will help you understand the relative noise between various CMOS bus-driver ICs.—*David Shear, Technical Editor*

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DESIGN FEATURES

Electro/93: The show, the products

Find out what's in store at the Northeast's largest electronics conference and convention.—*EDN Staff*

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Generalized op-amp model simplifies analysis of complex feedback schemes

When attempting to find a path through a forest of complex op-amp feedback arrangements, you can lose your way amidst all the branches on the trees. Consolidating the branches into standard blocks for a generalized op-amp model can help you forge a simple analysis path.—*Jerald Graeme, Burr-Brown Corp*

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Graft Windows programs to your custom software and reduce your workload

You can combine Windows programs with your own software to save time and effort when building complex, custom systems. Examples include using the spreadsheet Excel for data analysis and graphing, or, for drawing and graphing, word-processor Word for Windows.—*Bill Tolson, Hewlett-Packard Co*

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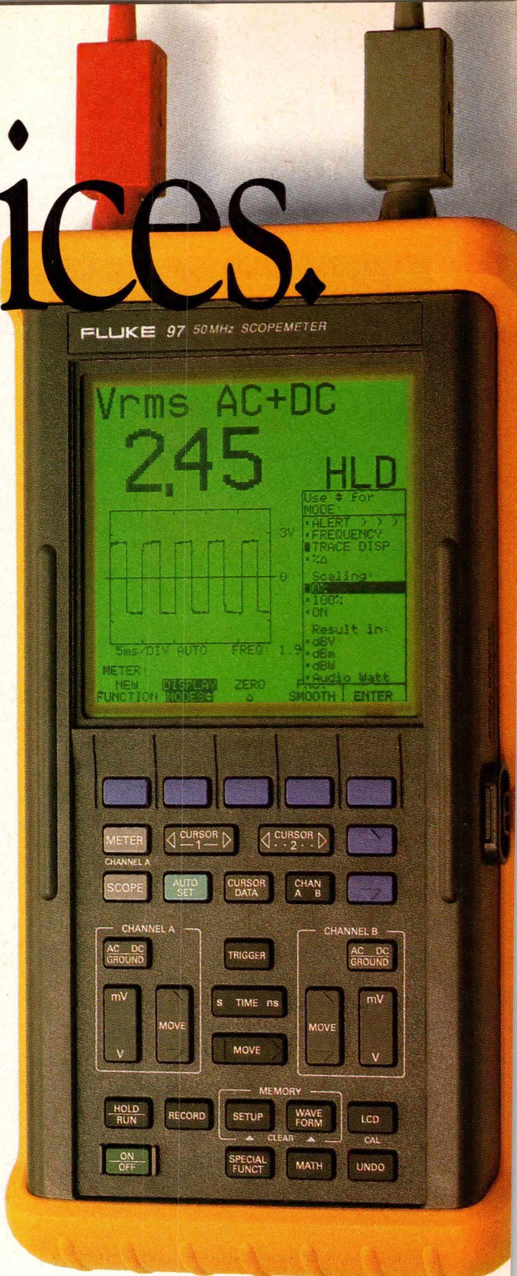

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CIRCLE NO. 4

EDN

April 15, 1993

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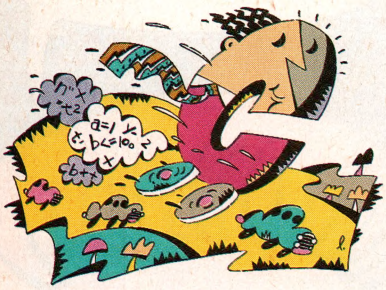

You can use C to speed up writing code, if you learn a few new tricks of the trade. By optimizing your code, you can write quick and concise C programs in a lot less time than you'd need to write them in assembler . . . . **PAGE 81**

TECHNOLOGY UPDATES

FPGA design services offer a helping hand

If you are unfamiliar with FPGAs, designing one on your own may be as inefficient as reinventing the wheel. Turning to an FPGA design expert can cut your development costs and speed your product to market. —*J D Mosley, Technical Editor*

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Design low-cost, quick-and-dirty applications with 8-bit μCs

You can do a lot with low-end 8-bit microcontrollers by creatively using their minimal memory, peripherals, and I/O pins.—*Ray Weiss, Technical Editor*

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Flash-memory ICs redefine program and data storage for portable applications

A single flash-memory chip can provide nonvolatile, updateable storage for execute-in-place program code. Multiple chips can create solid-state mass-storage systems.—*Gary Legg, Senior Technical Editor*

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Careful programming lets C replace assembler in fast embedded applications

You can break the assembler habit and still write fast, small embedded applications if you follow a few simple rules.—*John Donovan, Managing Editor, EDN Asia*

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EDITORIAL

Leave me alone

Personal communications may be a boon, but it can be a distraction and a headache, too.—*Jon Titus, Editor* **47**

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INSIDE EDN

A summary and analysis of articles in this issue

It's Electro time again, which offers some hope that spring has finally put an end to a long and snowy winter here in the Northeast. If you're planning to travel to Electro '93, however, don't worry about the weather in New York or Boston where the show has traditionally been held. But do bring along a road map: Electro is in Edison, New Jersey, this year. Check out **Electro/93: The show, the products** for a concise preview and round-up of the cutting-edge products featured at this year's show.

David Shear contributes this issue's Special Report, **EDN ground-bounce tests revisted**, which picks up where his original ground-bounce test project left off more than four years ago. This time, however, David has expanded his survey to accommodate a multitude of new products. "We originally tested 11 chips. This time we tested 72 chips, as well as nine package types." Because ground bounce can cause IC failure, intermittent system problems, and even the death of a product, David says it's critical to test whether ground bounce will affect your design.

This issue's four Technology Updates tackle FPGAs (field-programmable gate arrays), low-end 8-bit microcontrollers, flash-memory ICs and programming in C. JD Mosley's article on **FPGA design services** suggests that if you have little experience designing FPGAs, you may want to consider hiring someone to design for you. An FPGA expert may save you both time and money. She says that although there are plenty of software tools available today that help you program FPGAs, she cautions that "anyone can use the software, but few can create a masterpiece." JD presents the pros and cons of using a design service by interviewing those in the field who have experience—both good and bad—to share.

Ray Weiss, our µP/µC guru on the West Coast, presents a Technology Update on **designing low-cost applications with 8-bit µCs.** Ray reports that design EEs are scrambling to cut costs by finding the cheapest microcontroller suitable for the job, and then working to minimize power, board space, and support chips. He says, "You can do a lot with low-end, 8-bit microcontrollers by creatively using their minimal memory, peripherals, and I/O pins."

The third Technology Update covers **flash-memory ICs.** Gary Legg explains that new architectures for flash-memory ICs make it possible to implement solid-state mass storage and modifiable, execute-in-place program storage. Gary discusses the block-erase capability, which is common to all new architectures, and he compares chips that target program storage vs mass storage.

And for software buffs, the last Technology Update, **Careful programming lets C replace assembler in embedded applications**, comes to us from EDN Asia's Managing Editor John Donovan in Hong Kong. John's feature details the "subtle" difference between writing code fast and writing fast code. "Having a blazingly fast implementation of an inherently brute force approach just isn't good enough." John maintains that by carefully optimizing your code (and resorting to a few tricks), you can write C programs that are almost as tight and fast as those written in assembler—and in a lot less time.

Oh, and by the way, keep an eye out for EDN editors Jon Titus and Anne Swager who will be EDN's representatives at Electro '93.

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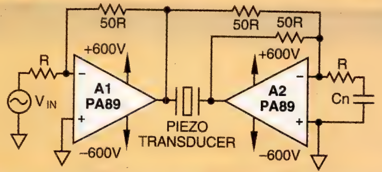
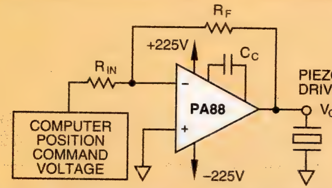
- 6.0mA max quiescent current



±1100V SINGLE AXIS MICRO-POSITIONING

PA88/PA88M—High Voltage, Low Quiescent Current

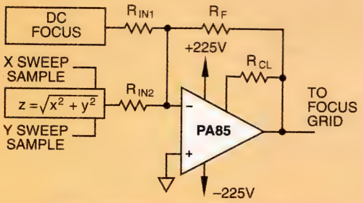
- ±225V supply
- 100mA output
- 2.0mA max quiescent current
- Programmable current limit
- High reliability, military version



±210V LOW POWER, PIEZOELECTRIC POSITIONING

PA85/PA85M—High Voltage, High Power Bandwidth

- ±225V supply
- 200mA output
- 550kHz power bandwidth
- 1000V/µs
- High reliability, military version



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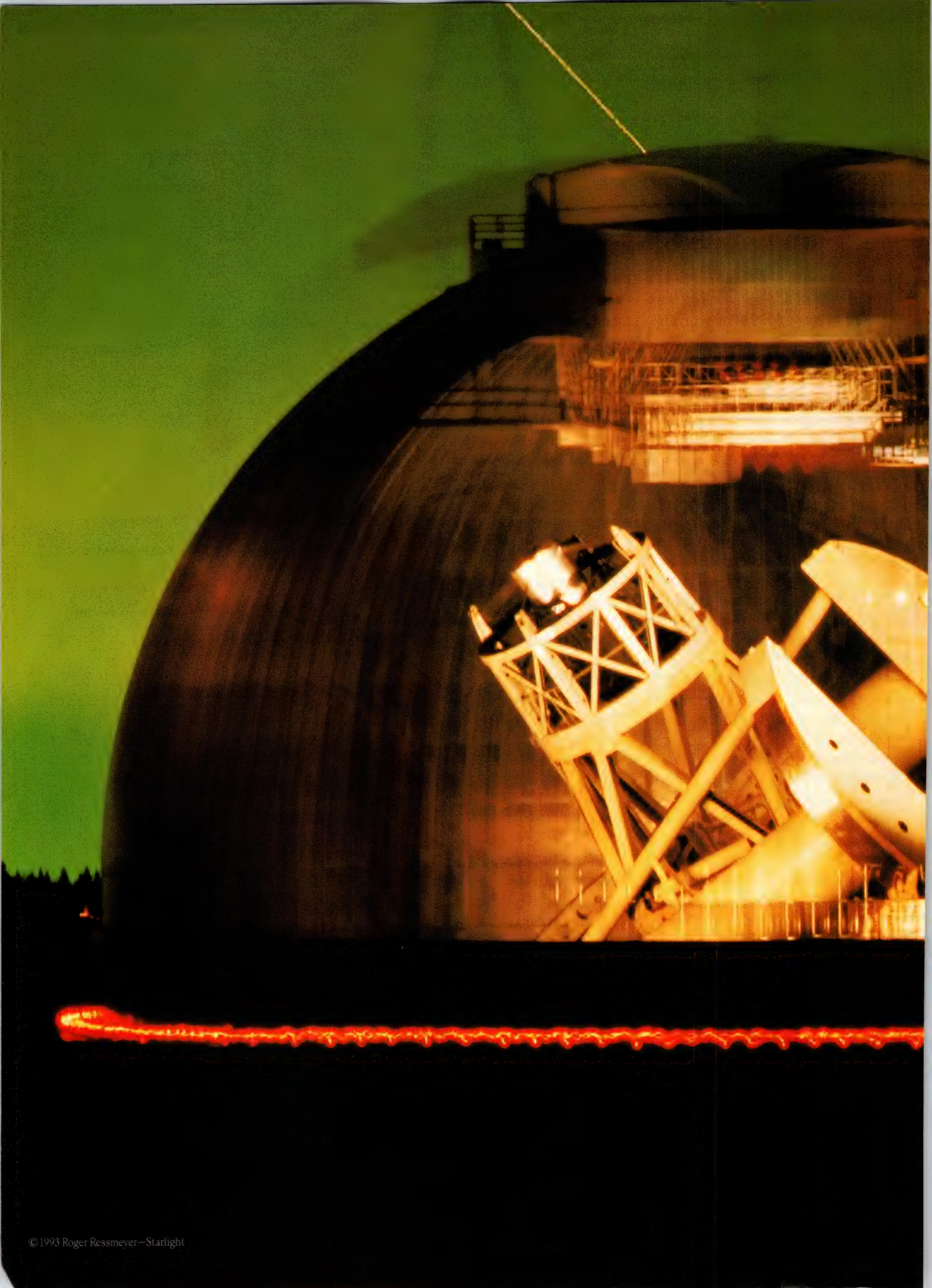

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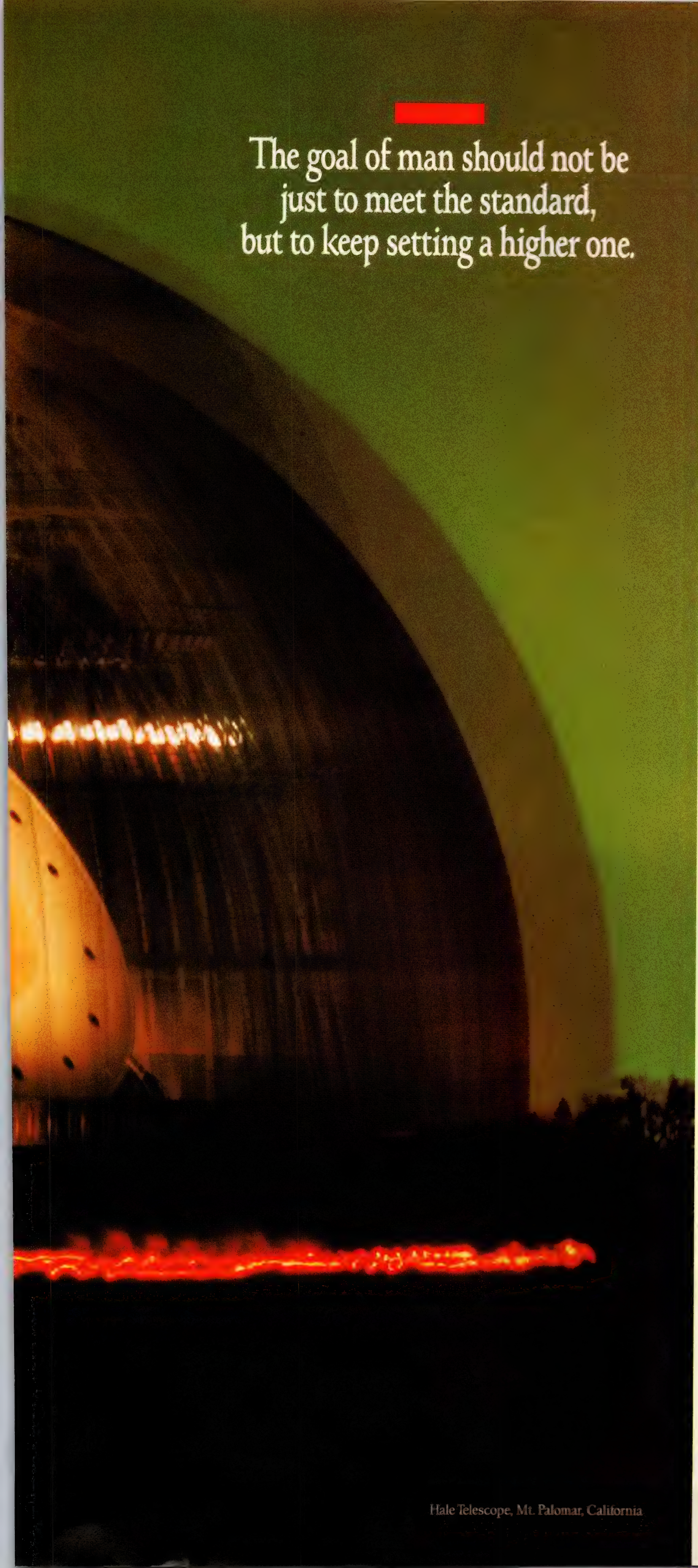

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just to meet the standard,
but to keep setting a higher one.

Hale Telescope, Mt. Palomar, California

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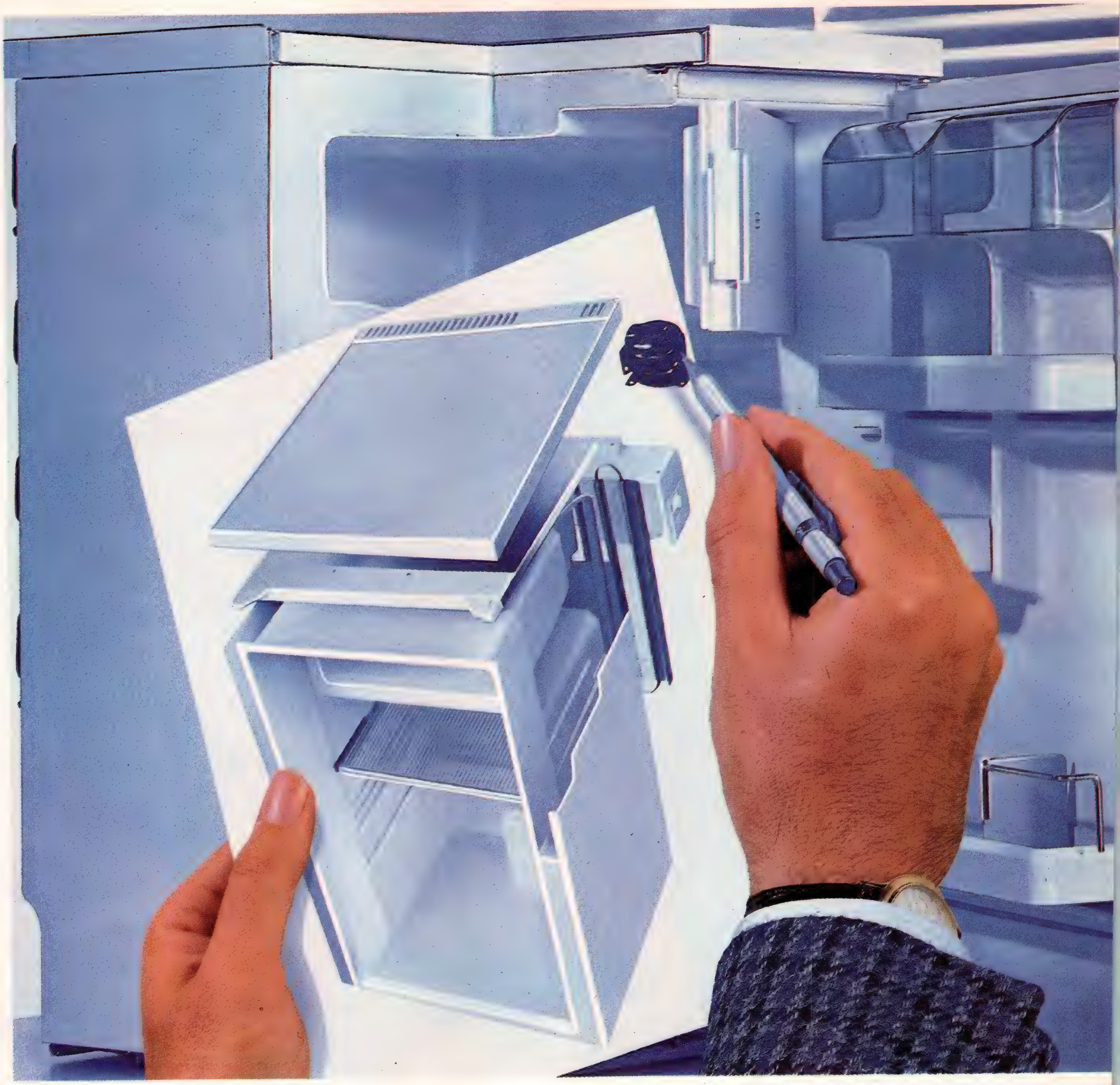

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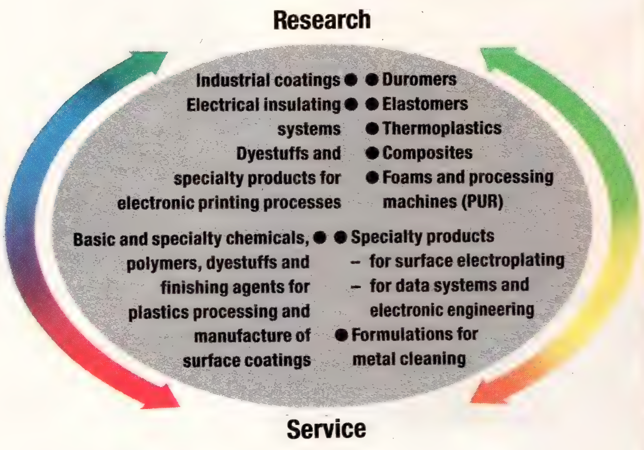
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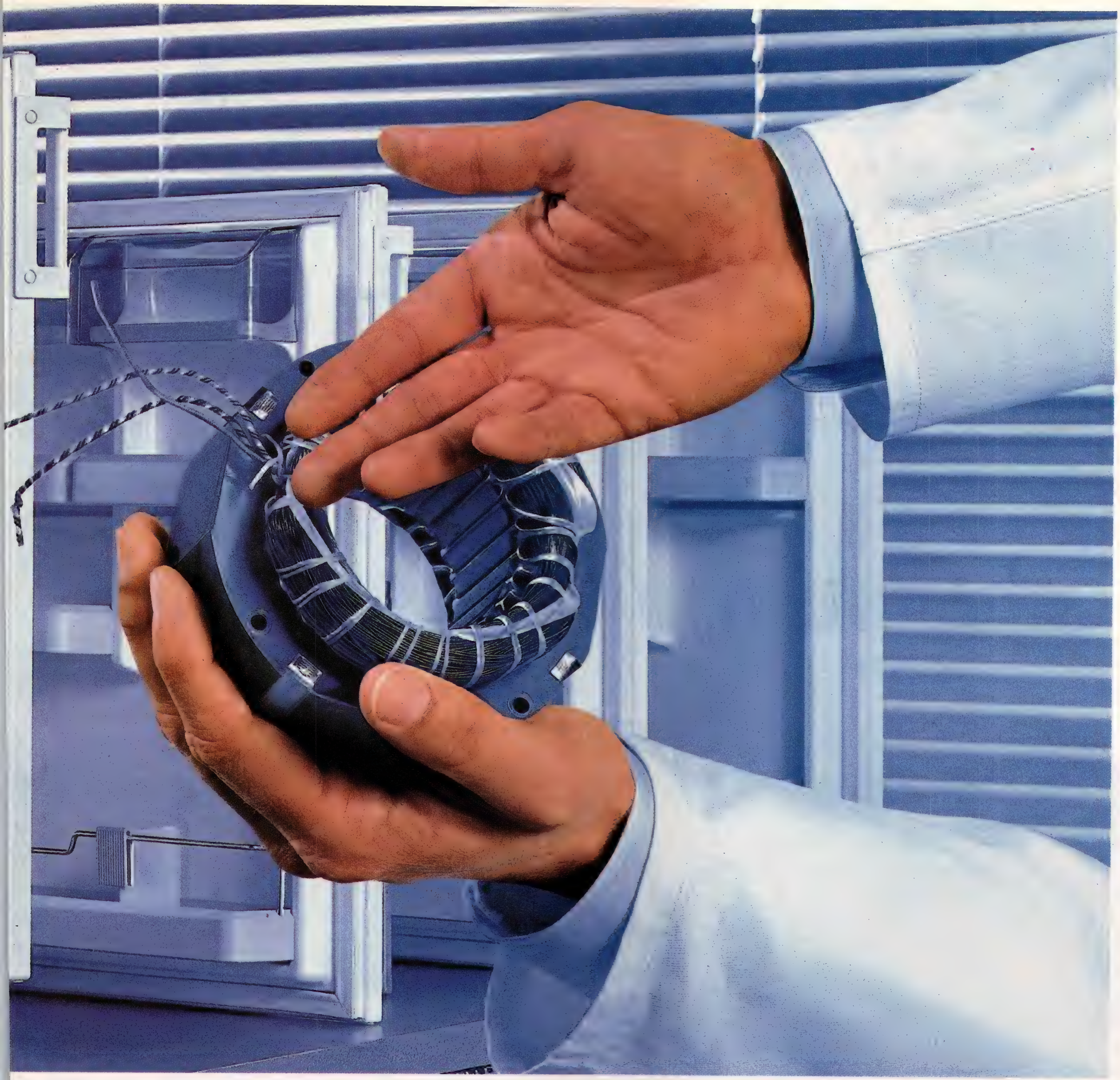
● Elastomers
● Thermoplastics
● Composites
● Foams and processing machines (PUR)
Basic and specialty chemicals, polymers, dyestuffs and finishing agents for plastics processing and manufacture of surface coatings ●
● Specialty products
– for surface electroplating
– for data systems and electronic engineering
● Formulations for metal cleaning
Service



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LeCroy 9210 300 MHz Programmable Pulse Generator

	with 9211 Module	with 9213 Module	with 9214 Module
TRANSITION SPEED	1 ns - 10 ms	6.5 ns - 95 ms	300 ps
MAX. REP. RATE	250 MHz	50 MHz	300 MHz
OUTPUT LEVEL	5V p-p (50Ω)	16V p-p (50Ω)	5V p-p (50Ω)
VARIABLE EDGES	Yes	Yes	No
TIMING ACCURACY	±(0.5% + 0.2 ns)	±(0.5% + 0.2 ns)	±(0.5% + 0.2 ns)

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Innovators in Instrumentation

CIRCLE NO. 15

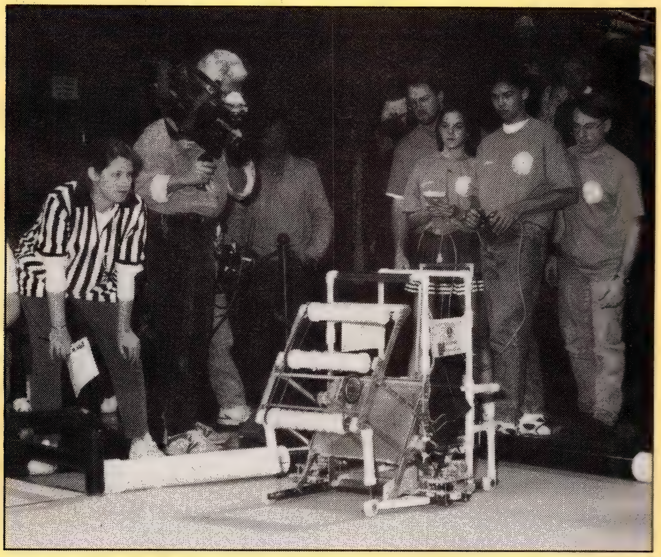
EDITED BY SUSAN ROSE

Students, practicing engineers join forces for design competition

US FIRST (For Inspiration and Recognition of Science and Technology) recently held its second annual design competition in Nashua, NH. Twenty-five teams made up of working engineers and high-school students received identical parts kits and designed radio-controlled robots that competed in elimination matches. On offense, a robot had to gather up water-filled kick balls and move them to an assigned corner; on defensive, the robot could do anything within its capabilities to stop another team from achieving the same goal. After a 2-day competition, the team of E-Systems/ Dallas Christian High School (TX) came away with the grand prize. Judges awarded AT&T Bell Labs/Newark Science High School (NJ) the Chairman's Award, given to the team that formed the most cooperative working relationship. The winners will be honored at a White House ceremony this spring.

Many other high-tech companies sponsored teams for the national competition, including Honeywell, Xerox, Boeing, Texas Instruments, Delco Electronics, Ford, and Lockheed. Motorola, which didn't field a team this year, nevertheless designed and donated the digital wireless controllers that gave the robots complete freedom of movement.

US FIRST, a nonprofit organization founded by inventor Dean Kamen, develops innovative programs to generate interest in science and technology among students. Any company that's interested in getting involved in next year's competition can select **Circle No. 571**, or contact the organization at 340 Commercial St, Manchester, NH 03101, (603) 666-3906, FAX (603) 624-0573.—by Joan Morrow Lynch



The E-Systems/Dallas Christian High School team rev up the winning robot in the second annual US FIRST design competition.

Firm offers lifetime use for FPGA tool

To entice new users, especially PAL designers, into trying field-programmable gate arrays (FPGAs), Actel is selling its Designer software tool for $995. The software supports all of the company's current devices with 2500 or fewer gates in the ACT 1, 2, and 3 families. What is unique about the offer, however, is that the company guarantees that the tool will be compatible with all of its future products that have 2500 or fewer gates. **Circle No. 564.** Actel Corp, Sunnyvale, CA, (408) 739-1010, FAX (408) 739-1540.

—by Doug Conner

Companies redesign erasable-PLD family

Altera Corp and Cypress Semiconductor are redesigning their programmable-logic family (called the MAX 5000 and CY7C34X, respectively) using a 0.65-μm process. The redesign will double the speed of the erasable-PLD family and reduce die size by 40%. Prototype devices are in test now; products should be available in the second half of 1993. Although the price has not been set, the companies anticipate a significant price reduction as a result of the die-size reduction. The new devices will be pin and software compatible with the existing family. **Circle No. 562.** Altera Corp, San Jose, CA, (408) 894-2800. Cypress Semiconductor Corp, San Jose, CA, (408) 943-2600. **Circle No. 563.**

—by Doug Conner

Chip set decodes MPEG TV in broadcast applications

The idea of having 500 television channels on a single cable-TV line may be appealing or appalling, depending on your attitude toward the medium, but it is rapidly becoming a technical probability. A collection of ICs from LSI Logic represents a large step in that direction by providing MPEG decoding capability for broadcast applications. The ICs, a video decoder, an audio decoder, and Reed-Solomon error-correction decoders, all work together with little additional logic.

The L64112 MPEG video decoder provides full CCIR601 images—720 × 480-pixel, 30 frames/sec NTSC and 720 × 576-pixel, 25 frames/sec PAL—from an MPEG1 bit stream. The IC also handles such nonvideo data as teletext, closed captioning, and anticopy coding. It accepts the MPEG bit stream directly from the video channel demodulator and feeds either progressive-scan or interlaced video data in YUV color format directly to a video converter for display. You need to add 16 Mbits of dynamic RAM (DRAM) for frame storage, but that's all; the chip has a built-in DRAM controller.

The L64111 MPEG audio decoder also accepts data directly from the channel demodulator, then extracts and decompresses the audio portion. It feeds the audio data directly to a DAC at rates as great as 384 kbps (stereo) with a sampling rate of 32 to 48 kHz. The L64111 uses an external 256k × 4-bit DRAM to buffer the audio data and coordinates audio/video synchronization with the video-decoder IC.

Broadcast transmissions are prone to error-inducing noise, so LSI Logic added Reed-Solomon error-correction devices to its chip set. Three device types are available, depending on the amount of correction your system needs. The L64712 corrects as many as five byte errors in a code block, the L64713 corrects ten, and the LR64714 corrects 16. An encoder IC, the L64711, provides all three formats. For the occasional burst error, the video and audio decoders offer error concealment.

All parts are available in sample quantities; full production is scheduled for the third quarter of 1993. In sample quantities, the L64112 video decoder costs $125, the L64111 audio decoder costs $35.95, the Reed-Solomon decoders start at $35, and the encoder costs $27 (1000). Prices decrease with large-volume purchases. **Circle No. 561.** LSI Logic, Milpitas, CA, (408) 433-8000, FAX (408) 433-7715.

—by Richard A Quinnell

Floorplanners move ASIC models closer to reality

Two recently introduced ASIC floorplanning packages move a long way toward reconciling preliminary timing simulations with real performance numbers. Design Planner 2.0 from High Level Design Systems nestles into the Cadence Design Framework and links to the associated tools. The floorplanner accepts logic designs from Cadence Edge or Composer schematics, Viewlogic's Powerview schematics, EDIF netlists, and several other netlist formats. The floorplanner automatically partitions flat netlists into blocks, based on wire-length and crossing-count criteria. Then automatic (or manual) block placers and prerouters create a design that a variety of timing simulators can use. The product accepts standard-cell, gate-array, and macrocell library information using the common GDS II format. An optional delay calculator can produce very accurate delay estimates more quickly than full simulation. Product licenses cost $25,000 to $60,000.

Similarly, Compass Design Automation's ChipPlanner, a part of the company's ASIC Navigator tool set, works with Cadence design tools and produces designs for several timing simulators. This product currently works with cell libraries from Hitachi, Raytheon, ES2/US2, and VLSI Technology. The floorplanner performs block placement from HDL descriptions and optimizes timing by incrementally exchanging cells with different drive strengths to achieve specified delays for critical nodes. This feature circumvents time-consuming synthesis iterations. Pricing starts at $30,000. **Circle No. 566.** Compass Design Automation, San Jose, CA, (408) 433-4880, FAX (408) 434-7820. **Circle No. 567.** High Level Design Systems, Santa Clara, CA, (408) 748-3456, FAX (408) 748-3499.

—by Steven H Leibson

Group supports standard industrial bus

Although it originated in Europe in 1989, the Process Field Bus (Profibus) is now in use in industrial controls and industrial-automation systems in the US, too. The Profibus is a part of the European universal fieldbus standard (DIN 19245) adopted in 1989. The US-based Profibus Trade Organization (PTO) aims to promote Profibus and disseminate information about the bus to designers and industrial-automation companies. The group supplies the standards for the bus-communication protocol, along with lists of manufacturers who support the bus with hardware and software. The bus uses a standard RS-485 serial link between controllers, actuators, sensors, and computers, so you don't need proprietary chips or software to adopt the bus. **Circle No. 570.** For more information, contact Mike Bryant, Profibus Trade Organization, Pittsburgh, PA, (412) 921-3322, FAX (412) 921-3356.—by Jon Titus

MicroSPARC architecture available for VMEbus

The SPARC 2LX computer from Themis Computer is the first VME product to use the MicroSPARC architecture. Delveloped under license from Sun Microsystems and based on a 50-MHz MicroSPARC (Tsunami) chip from Texas Instruments, the computer brings SPARCstation 2 performance (24 SPECmarks) to embedded systems. The MicroSPARC chip integrates

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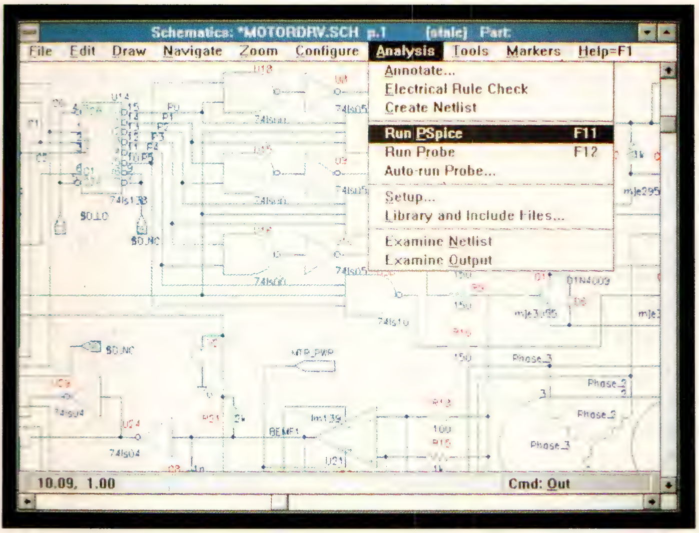

Schematic capture and PSpice simulation of a brushless DC motor

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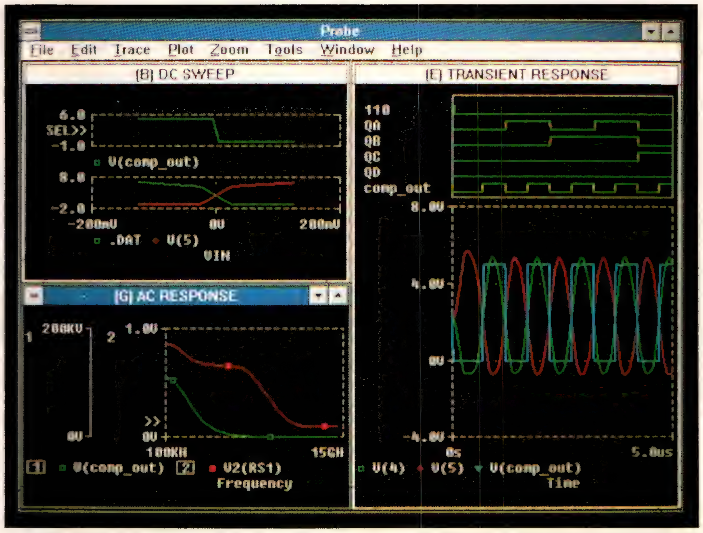

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The computer can run versions 1.x and 2.x of Sun's Solaris OS. Solaris 2.1 provides 500-µsec task switching. For faster real-time response, the computer can run Lynx Real Time Systems' LynxOS 2.0, with task switching of 200 µsec. Themis plans to have the computer also run VxWorks from Wind River Systems and OS-9000 from Microware Systems. The computer costs $3995 (100). **Circle No. 565.** Themis Computer, Pleasanton, CA, (510) 734-0870.—by Gary Legg

Pentium ICE makes debut

The LA/ICE-I5 provides real-time in-circuit emulation for Intel's recently announced Pentium µP. The ICE implements start/stop, breakpoint, and single-step operations using Pentium's built-in emulation features. The $11,995 product requires a PC and the company's logic analyzer. (For $32,975, you'll get the analyzer, too.) **Circle No. 569.** American Arium, Tustin, CA, (714) 731-1661, FAX (714) 731.
—by Steven H Leibson

ASIC design system integrates RF tools

Harris Semiconductor has integrated RF and IC design tools in the Fastrack design system for analog and mixed-signal ASICs. The system will be available in the August release of version 3.6. This system, and its links to Harris' IC fabrication processes, makes it possible to design and analyze ASICs that include RF circuitry. The system's RF library is based on the company's UHF-1 process, which boasts npn and pnp transistors with F_Ts of 8 and 5.5 GHz, respectively.

The RF tools include s-parameter modeling and simulation that support ac and nonlinear transient simulation; large-signal ac analysis; and RF-specific data representation and analysis, including Smith charts, polar plots, intermodulation plots, windowed FFTs, large- and small-signal distortion analysis, and noise figure. To create the embedded RF tools, the company enhanced and modified the system's Cadence IC framework, Cadence Spice, and data-analysis tools.

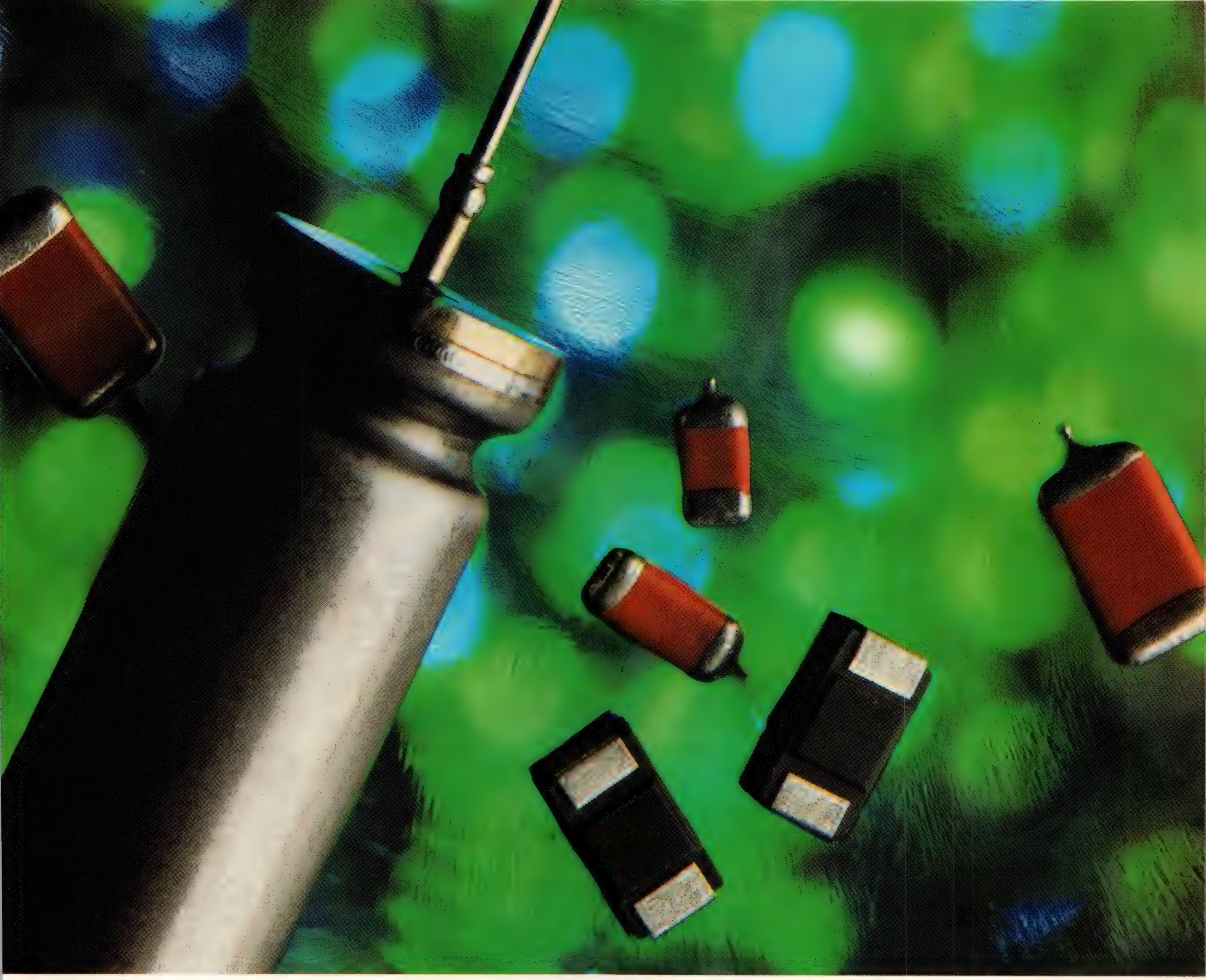
Integrating the noise and RF data-analysis tools was straightforward, but including large-signal ac analysis and s-parameter modeling took extensive modification and enhancements to the simulation engine and user interface. Release 3.6 of Fastrack will run on Sun SPARC 2 and SPARC 10 workstations. Pricing will depend on configuration but will begin at $31,000 for analog-only applications. **Circle No. 572.** Harris Semiconductor, Melbourne, FL, (800) 442-7747, ext 7084.
—by Anne Watson Swager

Newly formed corporation pushes PowerPC

Seven vendors have announced the PowerOpen Association, a corporation to create and certify compliance with standards for the PowerPC RISC µP family. The founding companies are Apple Computer, Bull, Harris, IBM, Motorola, Tadpole Technology, and Thomson-CSF. Domenic LaCava, formerly Digital Equipment Corp's RISC guru, is the corporation's president. The corporation has been operating for 18 months and will soon complete an application-binary-interface (ABI) specification that will let the same software run on all PowerOpen machines, ranging from battery-powered portable computers to multiprocessor mainframes. A "shrink-wrapped" software standard is the only way a computer platform can achieve broad market acceptance in the 1990s. As the originators of the µP architecture, Motorola, IBM, and Apple are determined to ensure that the PowerPC becomes successful. The PowerOpen ABI is based on IBM's AIX/6000 Unix variant, the OSF/Motif graphical user interface, and Apple's Macintosh user interface. **Circle No. 568.** PowerOpen Association, Billerica, MA, (508) 294-4540, FAX (508) 294-4585.
—by Steven H Leibson

Judge rules firms infringed on patent

An International Trade Commission judge has ruled that two Taiwanese semiconductor companies have been unlawfully importing dialer chips that infringe on an SGS-Thomson patent. The two companies are Hualon Microelectronics Corp and United Microelectronics Co. SGS-Thomson stated that based upon this ruling, it would seek an order excluding the dialer chips, as well as telephones and other devices containing them, from being imported into the United States. According to the company, such an exclusion order would not affect Winbond Corp of Taiwan's products because the company has recently obtained Taiwanese government approval of a cross license with SGS-Thomson. **Circle No. 575.** SGS-Thomson, Carrollton, TX, (602) 867-6259, FAX (602) 867-6102.
—by Susan Rose



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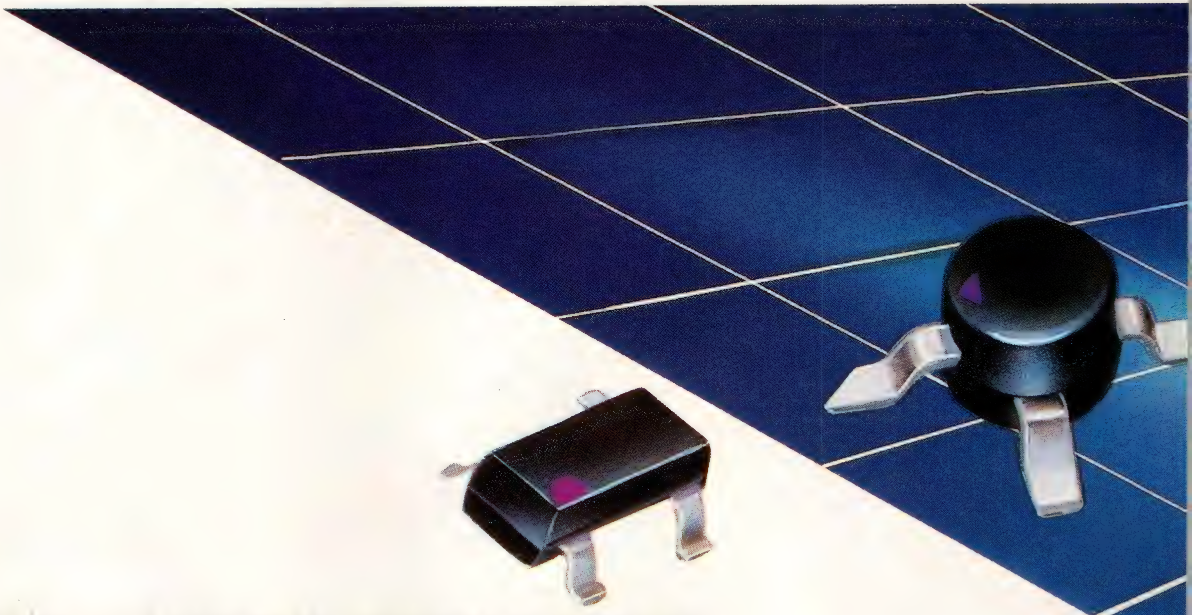

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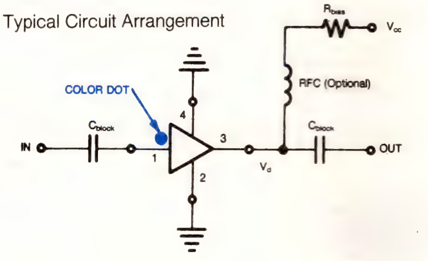
Typical Circuit Arrangement



SPECIFICATIONS

Model No.	Freq.,MHz dc to:	Gain,dB 100 MHz	Output Pwr +dBm	NF dB	High Gain (features)	Power (features)	Low Noise (features)	Price, $ ea. (25 Qty)
SURFACE MOUNT								
MAR-1SM	1000	18.5	1.5	5.5	●			1.04
MAR-2SM	2000	12.5	4.5	6.5				1.40
MAR-3SM	2000	12.5	10.0	6.0				1.50
MAR-4SM	1000	8.3	12.5	7.0		●		1.60
MAR-6SM	2000	20.0	2.0	3.0	●		●	1.34
MAR-7SM	2000	13.5	5.5	5.0				1.80
MAR-8SM	1000	32.5	12.5	3.3	●	●	●	1.75
MAV-1SM	1000	18.5	1.5	5.5	●			1.15
MAV-2SM	1500	12.5	4.5	6.5				1.45
MAV-3SM	1500	12.5	10.0	6.0				1.55
MAV-4SM	1000	8.3	11.5	7.0				1.65
MAV-11SM	1000	12.7	17.5	3.6		●	●	2.15
VAM-3	2000	11.5	9.0	6.0				1.45
VAM-6	2000	19.5	2.0	3.0	●		●	1.29
VAM-7	2000	13.0	5.5	5.0				1.75
HERMETICALLY-SEALED SURFACE MOUNT								
RAM-1	1000	19.0	1.5	5.5	●			4.95
RAM-2	2000	12.5	4.5	6.5				4.95
RAM-3	2000	12.5	10.0	6.0				4.95
RAM-4	1000	8.5	12.5	6.5		●		4.95
RAM-6	2000	20.0	2.0	2.8	●		●	4.95
RAM-7	2000	13.5	5.5	4.5				4.95
RAM-8	1000	32.5	12.5	3.0	●	●	●	4.95
FLATPACK								
MAR-1	1000	18.5	1.5	5.5	●			0.99
MAR-2	2000	12.5	4.5	6.5				1.35
MAR-3	2000	12.5	10.0	6.0				1.45
MAR-4	1000	8.3	12.5	6.5		●		1.55
MAR-6	2000	20.0	2.0	3.0	●		●	1.29
MAR-7	2000	13.5	5.5	5.0				1.75
MAR-8	1000	32.5	12.5	3.3	●	●	●	1.70
MAV-1	1000	18.5	1.5	5.5	●			1.10
MAV-2	1500	12.5	4.5	6.5				1.40
MAV-3	1500	12.5	10.0	6.0				1.50
MAV-4	1000	8.3	11.5	7.0				1.60
MAV-11	1000	12.7	17.5	3.6		●	●	2.10

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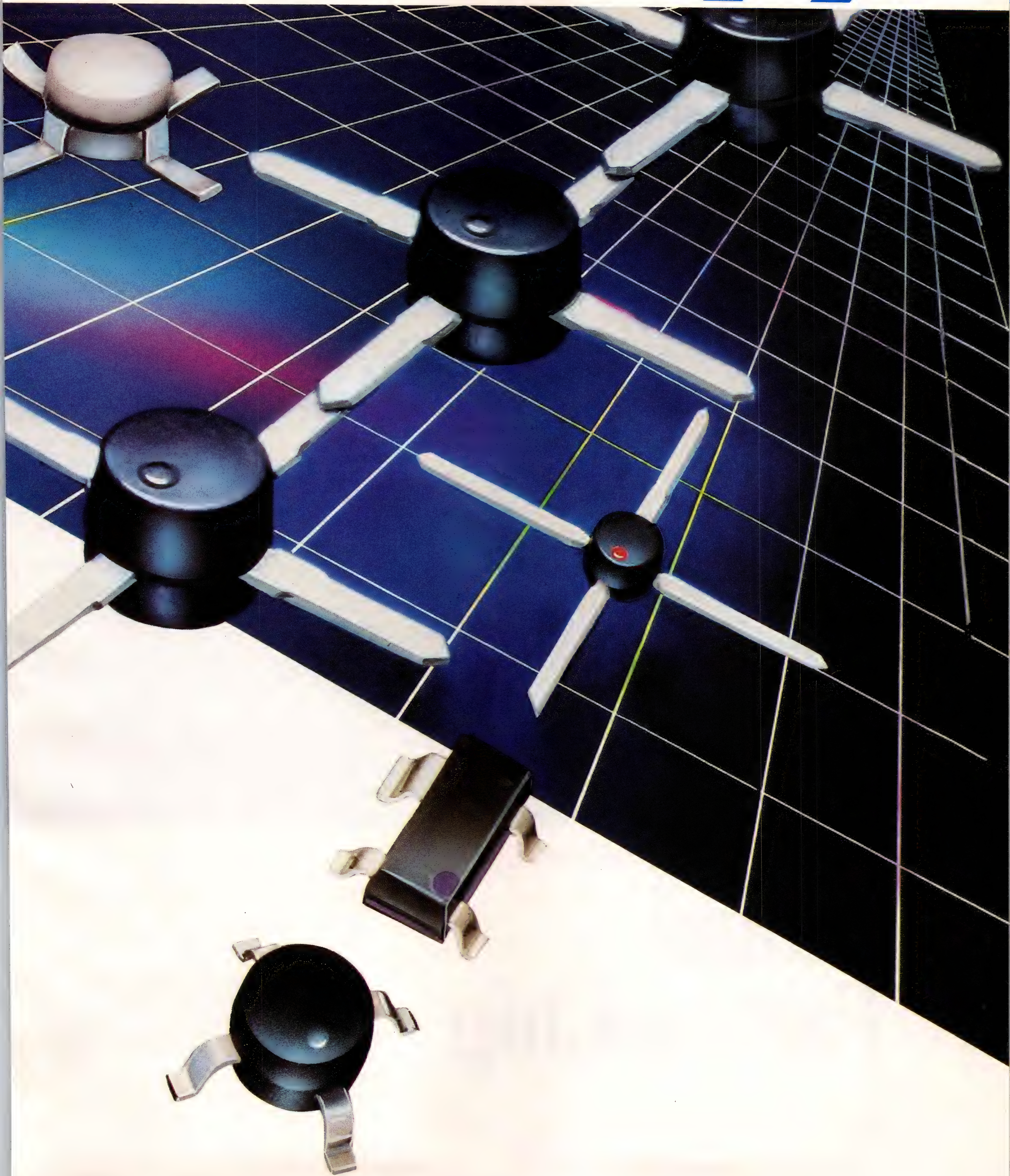

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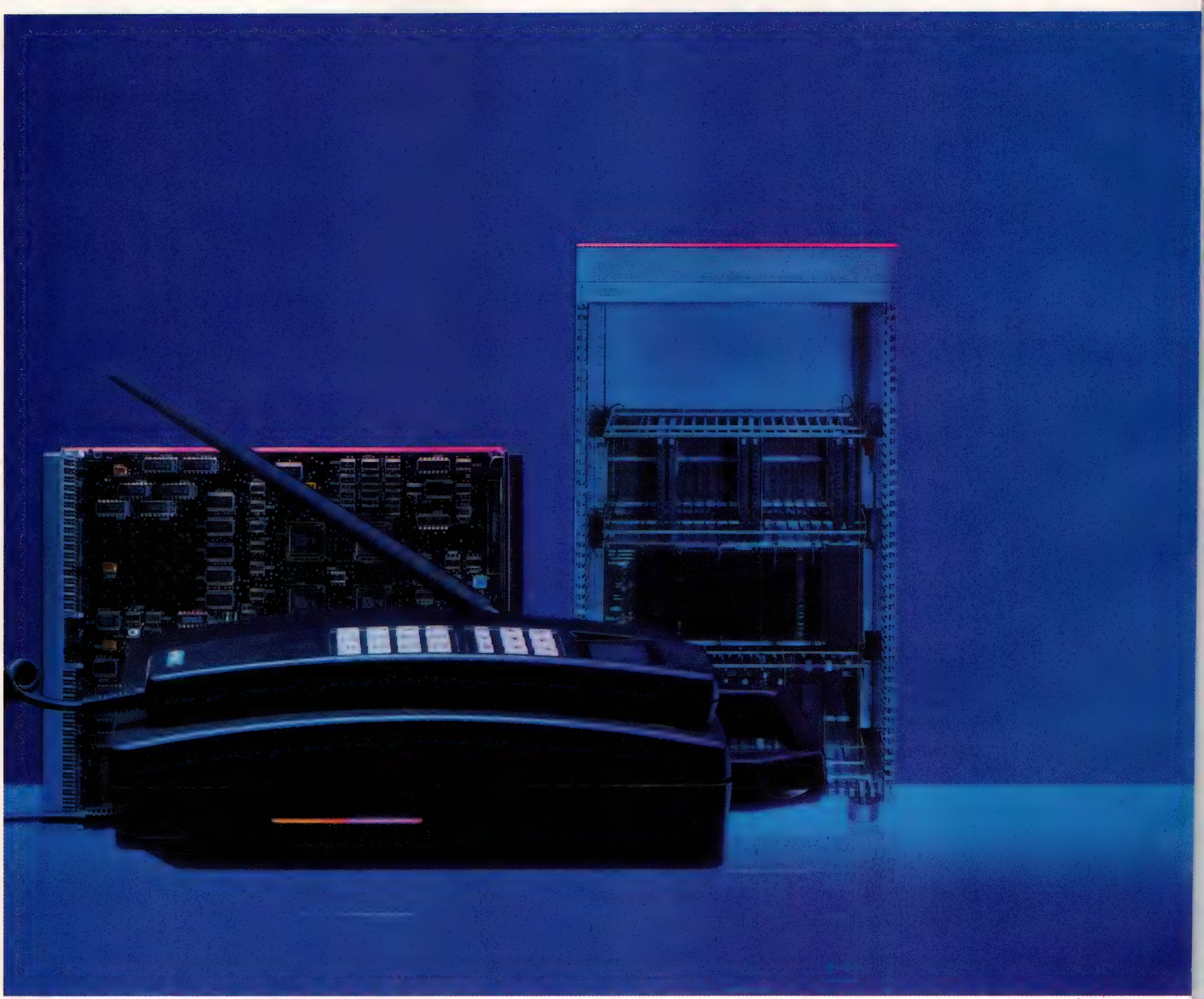

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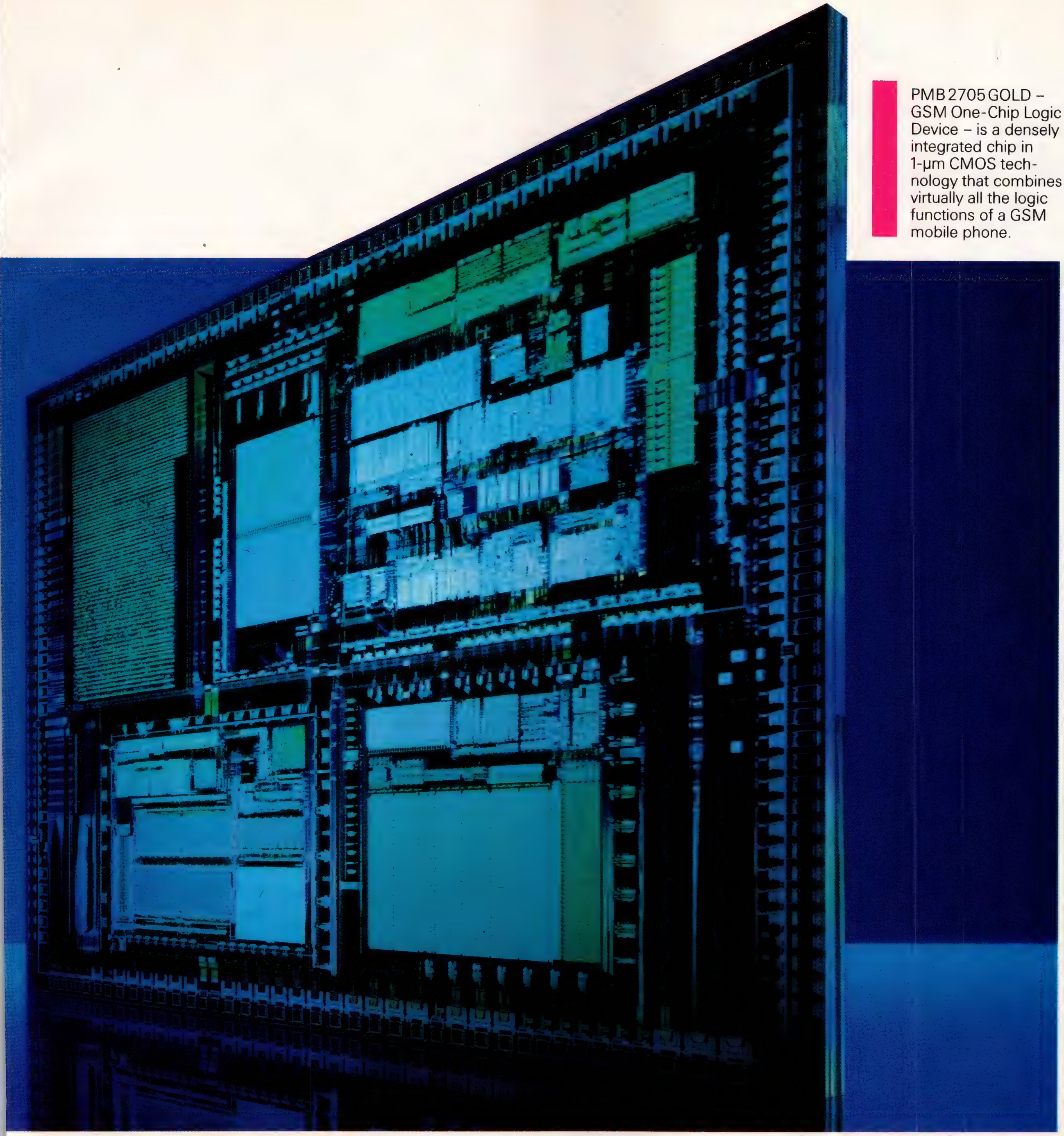

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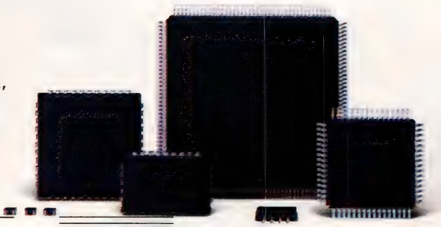

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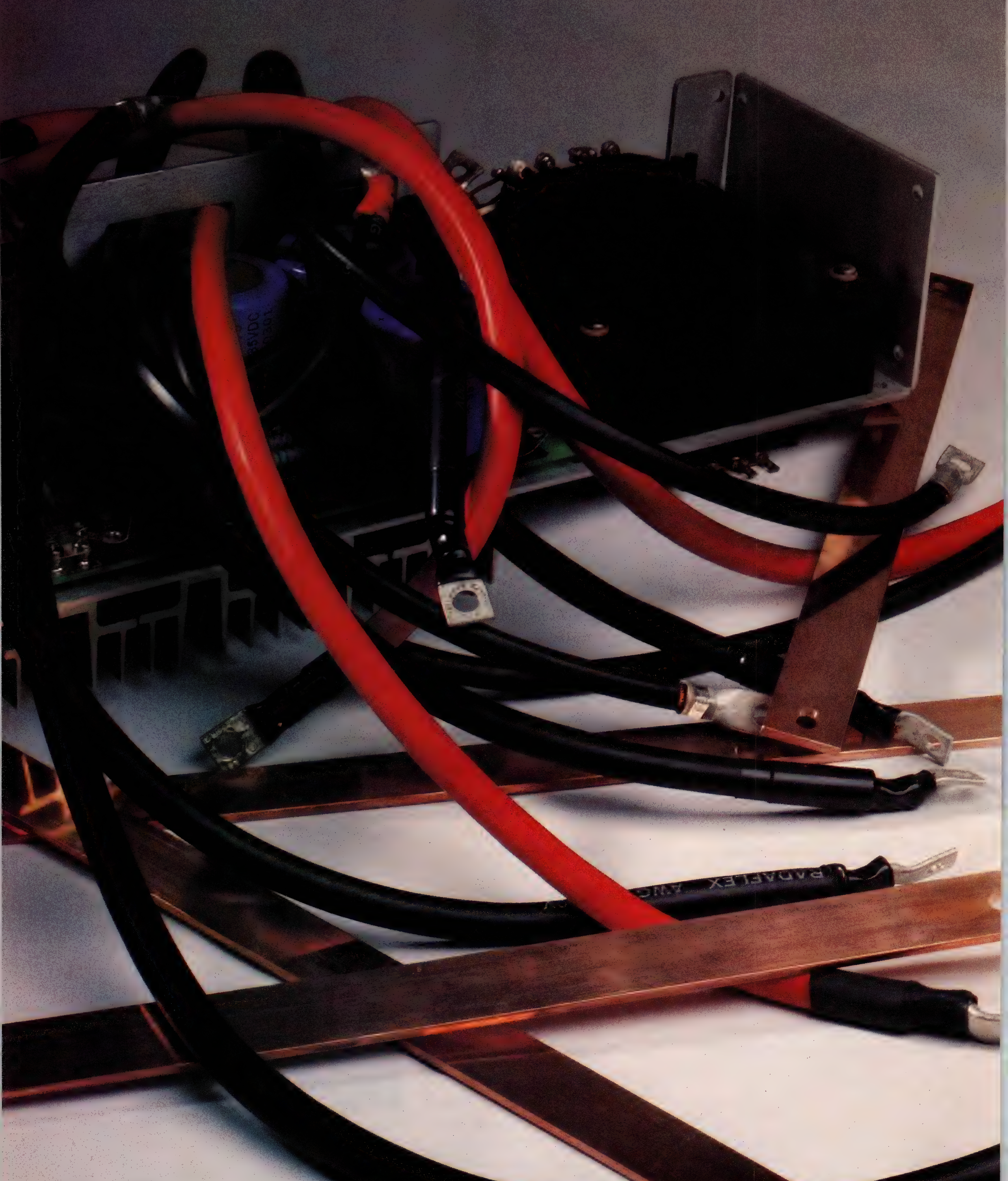

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The changing world of PLDs and FPGAs

Congratulations on producing one of the best reviews yet of the tradeoffs involved in selecting a programmable ASIC ("Choosing complex PLDs and FPGAs," EDN, September 17, 1992, pg 74). Anne Watson Swager presents a concise summary of a complex issue in straightforward and easy-to-understand language.

She describes in the text, and shows graphically in Fig 3, how recent architectural developments are blurring differences in the efficiency of logic implementation between PLDs and FPGAs (field-programmable gate arrays). However, on pg 81, she reports the state of the art in performance predictability as it existed several years ago. In those days, PLD operating speeds were easy to predict. Static-RAM-based FPGAs, the only types available at the time, were indeed almost impossible to predict due to nondeterministic routing delays.

Two important factors have changed this simplistic view. New large complex PLDs use a variety of segmenting schemes to increase density. Most of these decrease timing predictability and routability, as they present a wide selection of possible implementations for the software tools to evaluate, and the designer cannot know in advance which alternative will be chosen. At the same time, metal-to-metal antifuse technologies are delivering FPGAs with very low impedance interconnect structures. These ensure that, as with PLDs, FPGA interconnect delays can now be shorter than logic-cell delays. Thus, while complex PLDs are increasing in density, in many applications they are now little more predictable than modern FPGAs, and a lot less flexible.

In a recent evaluation of FPGA capability, we automatically placed and routed a function that used every single logic cell and 75% of the I/O pins. It ran at 95 MHz. To determine the impact on performance of such high utilization, we eliminated 20% of the logic. The speed only improved to 98 MHz, proving that routing congestion is no longer the limiting factor for FPGAs. This is significantly different from the situation of just a couple of years ago and illustrates the dramatic progress that continues to be made in this exciting product area.

David A Laws, President
Quicklogic Corp
Santa Clara, CA

Testing electromagnetic immunity of products

Regarding the very interesting article, "EMC bench tools" (EDN, October 1, 1992, pg 78), I would like to comment on the method of testing the electromagnetic immunity of products. The conclusion of the article was that the only means for testing the immunity is the use of an ESD gun. In my experience, I have found another solution for testing immunity: The use of Standard IEC 801-4, "Electromagnetic compatibility for industrial process measurement and control equipment, Part 4, Electrical fast-transient/burst requirements."

In my opinion, the tests described in this standard are very useful for defining the *level* of immunity of your product; the ESD test always results in either the GO or the NO-GO type.

Fulvio Baratella
Fimet Motori & Riduttori
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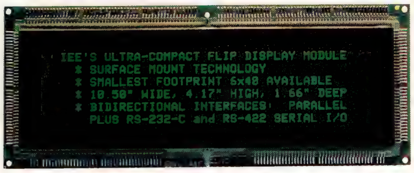
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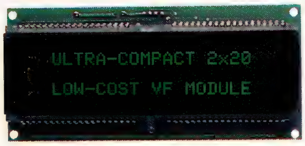

- The **NO-FRILLS™** and **NINETY SERIES™** are IEE's **low-cost VFDs** with a high-priced appearance and are ideal for OEM applications such as copiers, POS terminals, pay telephones, etc.

- **"Industrial Strength" FLIPs** feature 9, 11, and 15mm characters, making them easy to read from longer distances—typical on factory floor and in PLC applications.

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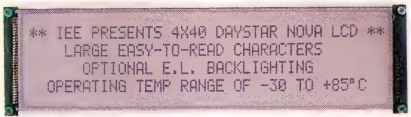
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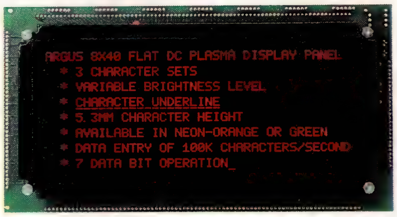
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- The **ARGUS™** line offers flicker-free DC plasma flat panel technology with character fields up to 480, in widths up to 40 characters. ARGUS eliminates the need for bulky CRTs.

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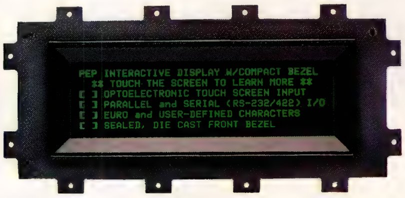
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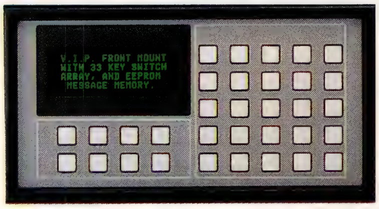

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The REMARKABLY DENSE ARGUMENT FOR THE CROSSPOINT FPGA.

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useable gates on one 12K chip.

Field Programmable Gate Arrays have always been a promising sort of product. But they haven't had nearly enough useable gates. Not to mention their pitifully low performance. And as a

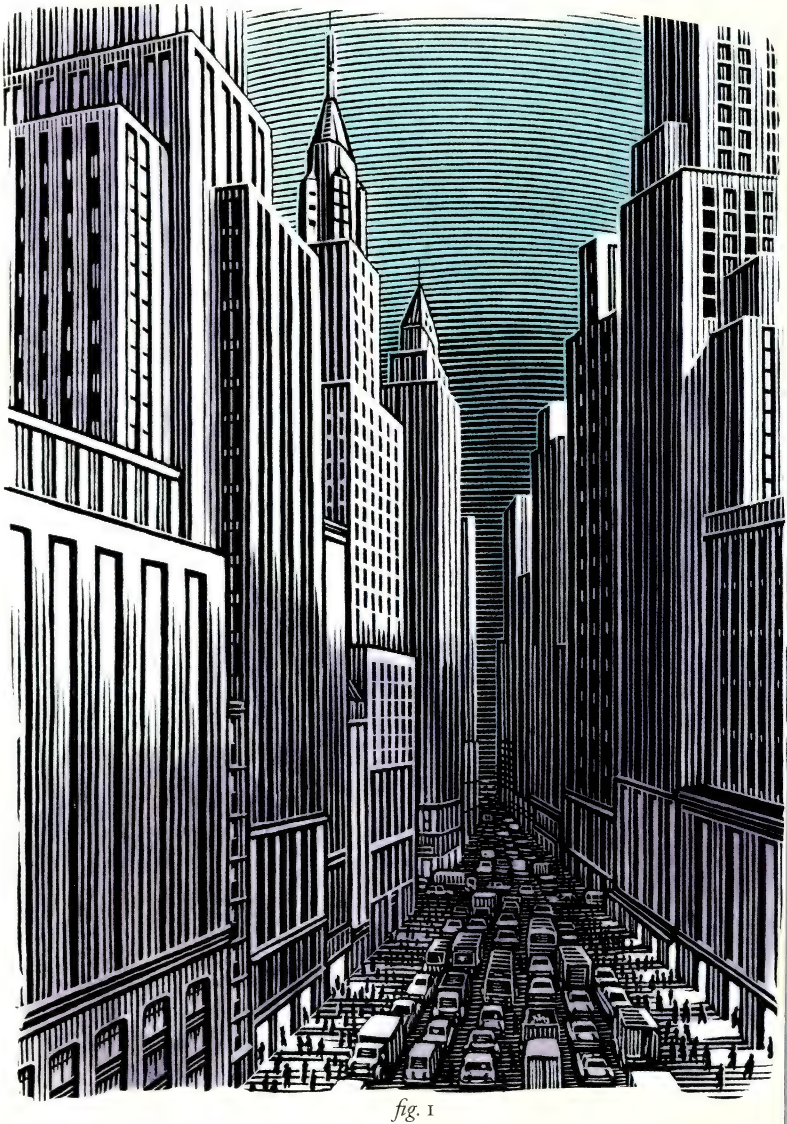


fig. 1

The Real World

It's a nasty, demanding place. Now there's an FPGA *with enough density to let you build the mainstream products that are used in it.*

result, the ASIC designer has seldom bothered with them. The Crosspoint FPGA is

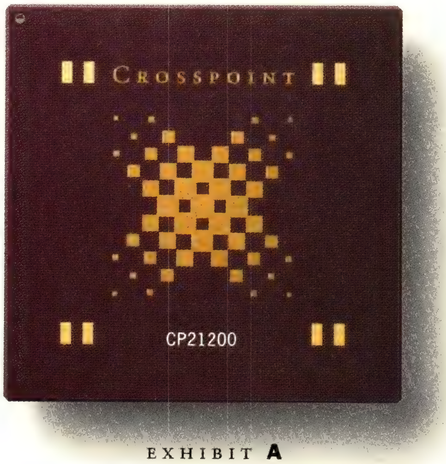


EXHIBIT **A**
The product. In through-hole.

a dream product that breaks all this wide open. It offers up to 10,000 true, useable gates on one 12K chip, and it's fast. Will it change design permanently?

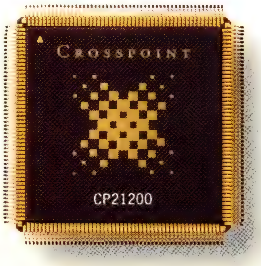


EXHIBIT **B**
The product. In surface mount.

We submit that it will.

In name, it's a 12K. But it gives you far more useable gates than that suggests. It's also fast. And predictable. All in all, a lot like a gate array. There's a reason.

IT *Is* A GATE ARRAY

Crosspoint gives you the industry's first 12K FPGA. But there's considerably more to it than that.

And, at the same time, less.

The Crosspoint FPGA offers unheard-of gate-utilization efficiency. The highest-available FPGA performance. And remarkable predictability with both.

All for one simple reason. Unlike *all other* FPGAs, Crosspoint's is—architecturally—a gate array.

Like a mask-programmable gate array, it has transistor-level granularity. And unlike previous FPGAs, it has gates.

Which, in itself, is noteworthy.

The smallest building blocks of all previous FPGAs are elaborate and complicated constructions—incorporating numerous logic macrocells with numerous functions. And resulting in an extremely complex chip for a rather modest number of "gates."

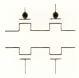


EXHIBIT **C**

Simplicity itself: our gate.

The smallest building block of the Crosspoint FPGA is something far simpler—a gate. A real one.

And that, in turn, is why our "12K" chip actually is a 12K—and gives you up to 10,000 useable gates— 10,000 *true,* gate-array gates. Which is a gate-utilization efficiency of up to 85%. Efficiency comparable to that of other true gate arrays. And, of course, far in excess

Crosspoint Solutions Incorporated

of what you get from existing FPGAS.

Our superior *performance* is also due to our streamlined architecture. We function in systems with clock speeds up to 50 Mhz. Which may not seem altogether meaningful in the murky environment of FPGA performance claims. But is very meaningful when you consider that *other* FPGAS will only function in systems in the 15-30 Mhz range.

fig. 2

Duck

There's an old saying: If it looks like a duck, and acts like a duck, it must be a duck. Our FPGA *acts like a gate array, and is one.*

The *predictability* of the Crosspoint FPGA is significant in itself. As with a gate array, you'll know what size circuit you can fit on the chip, and what speed it will operate at. So you'll know you aren't just spinning your wheels.

And we also give you built-in testability logic, per the JTAG Boundary Scan Architecture Standard—which will make board testing painless, and assure high quality.

At a glance, that's what the product is — technically.

What it *means,* is that for the first time you've got the FPGA you need. One without limitations, that will let you use FPGAs where you'd like to. In real-world products.

We'll also give you something else you can only get with a true gate array (and we think you'll especially appreciate our tools).

THE POWER *of* LOGIC SYNTHESIS.

Because of its gate array architecture, the Crosspoint FPGA is a perfect fit in the ASIC design environment.

It makes the cumbersome design methodology you associate with FPGAs, entirely a thing of the past.

For instance, Crosspoint's is the first FPGA that makes it viable to take advantage of logic synthesis, and use it to boost productivity.

The coarse granularity of previous FPGAs has made *using* logic synthesis so inefficient that there's been very little reason to do it. By contrast, the transistor-level granularity of the Crosspoint FPGA makes logic synthesis as efficient as it is with *any* ASIC.

Which is significant, because the extremely high useable-gate count that Crosspoint offers means there are big gains to be realized *with* logic synthesis.

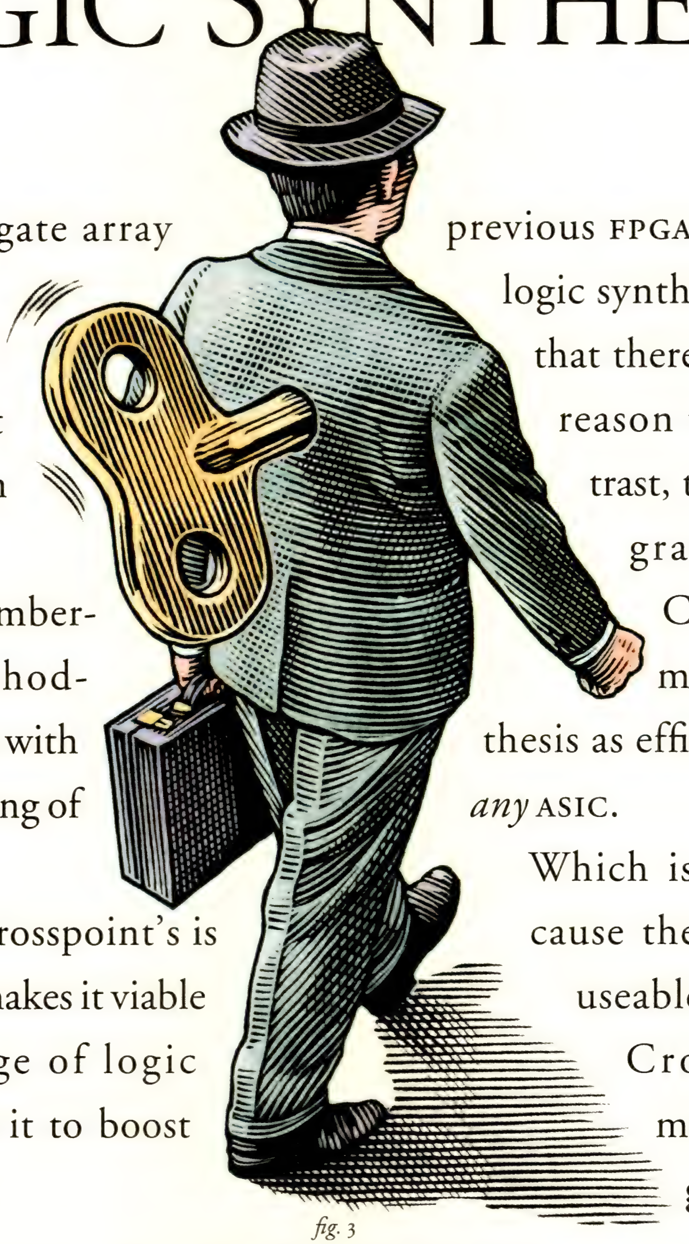
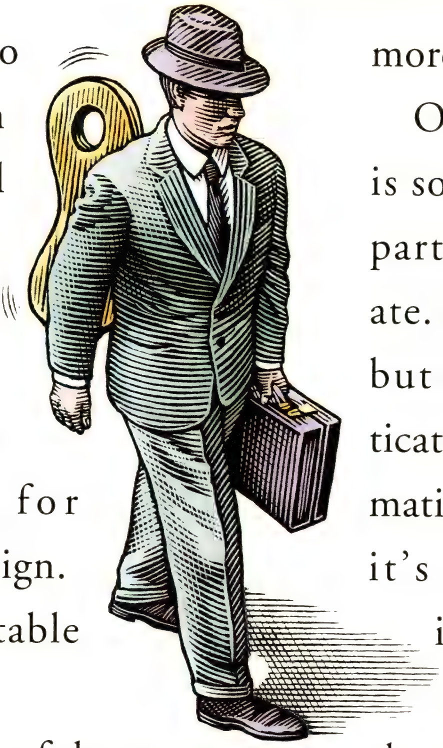


fig. 3

Your Own Automated Designer

You don't have to use logic synthesis, but there's a good reason to. Productivity. It's like having a clone of yourself. He excels at details and will go right where you point him.



When it comes to the rest of design automation, you'll be able to use the tools you're familiar with. In precisely the ways you use them for standard ASIC design. And with predictable results.

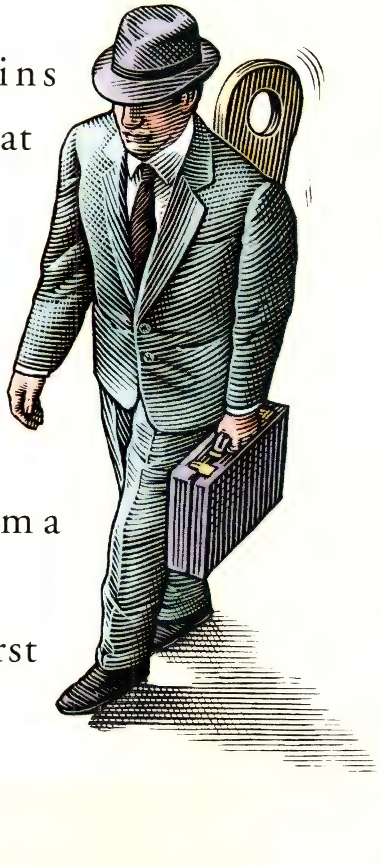
It is, in fact, one of the most important advantages we offer.

You'll find you can do both pre- and post-layout simulation. You'll have the familiar and efficient back-annotation path you expect with a gate array—something that's never previously been available for an FPGA.

And that will be true for any leading simulation product you work with. Crosspoint's Design Kits support the simulation, logic synthesis, schematic capture, and timing- and fault-analysis products of Mentor Graphics, Synopsys, Cadence/Verilog, Viewlogic. And more soon.

Our place & route is something you'll particularly appreciate. It not only *works,* but it's highly sophisticated. It's powerful, it's automatic, it's flexible, it's timing-driven, it's intuitive. And it offers an interactive editing capability that will help you fine-tune, if you choose to.

All in all, we've been careful to give you the tools that will make it not only feasible, but *easy* to realize the major gains that the Crosspoint FPGA allows for.



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EDITED BY JULIE ANNE SCHOFIELD

Books can help defense companies compete commercially

I read Jon Titus's editorial in the January 21, 1993, EDN (pg 27) and agree wholeheartedly. My company, EG&G Special Projects, is struggling to make the transition from Department of Defense contracting to competing in the commercial world and is looking for pointers. In his editorial, Jon mentioned that there are some good non-textbook sources for marketing information. Could you list some books to start with? EG&G's skills are in systems design and integration and low-volume/high-value electronic data-acquisition instruments.

Dave Thomson
EG&G Special Projects
Albuquerque Operations
Albuquerque, NM

Two good books are

Marketing High Technology, by William H Davidow, The Free Press (Division of Macmillan), New York, NY, 1986, ISBN 0-02-907990X, $23.95.

The Macintosh Way, by Guy Kawasaki, Scott, Foresman and Co, Glenview, IL, 1990, ISBN 0-673-46175-0, $19.95.

The Davidow book is a bit old, but it still contains useful information. A bookstore with a good management/business section should also have some practical marketing books.

EDN book series includes Pease and lots more

Where can I obtain a copy of the book *Troubleshooting Analog Circuits* by Robert A Pease? I understand the book contains material originally published in EDN. I've called several local bookstores, but to no avail.

Andy Walsh
Benthos Inc
North Falmouth, MA

Bob Pease's book is just one of the 10 books that makes up The EDN Series for Design Engineers. The books in the series are:

- *Analog Circuit Design: Art, Science, Personalities*, edited by Jim Williams, Linear Technology Corp, 1991, 352 pgs, $44.95.
- *Electronic Circuits, Systems & Standards*, edited by Ian Hickman, 1991, 256 pgs, $32.95.
- *EMC for Product Designers*, by Tim Williams, 1992, 272 pgs, $42.95.
- *Integrated Circuit and Waveform Generator Handbook*, by R M Marston, 1991, 267 pgs, $22.95.
- *Newnes Electronic Circuits Pocket Book*, by R M Marston, 1991, 344 pgs, $26.95.
- *Operational Amplifiers, Second Edition*, by Jiri Dostál, Research Institute for Mathematical Machines, Czechoslovakia, 1993, 360 pgs, $49.95.
- *Passive Components: A User's Guide*, by Ian Sinclair, 1990, 176 pgs, $21.95.
- *Radio Frequency Transistors: Principles and Practical Applications*, by Norman E Dye and Helge O Granberg, Motorola Inc, 1993, 228 pgs, $39.95.
- *Rechargeable Batteries Applications Handbook*, by the Technical Staff of Gates Energy Products, 1992, 432 pgs, $49.95.
- *Troubleshooting Analog Circuits*, by Robert A Pease, National Semiconductor Corp, 1991, 208 pgs, $32.95.

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Transformer makers come to light

In the October 29, 1992 edition of EDN, I found the article "Designing supplies for powering LCD backlighting" by Jim Williams very useful. I am trying to contact the manufacturers of the transformers specified in the article—Coiltronics and Sumida—or their US distributors. Can you help?

Mark Godfrey
Hunting Avionics Ltd
Uxbridge, UK

Coiltronics
984 SW 13th Ct
Pompano Beach, FL 33069
(305) 781-8900
FAX (305) 781-8703

Sumida
637 E Golf Rd, Suite 209
Arlington Heights, IL 60005
(708) 956-0666
FAX (708) 956-0702

Rochester Electronics to acquire discontinued AMD parts

If you're looking for or currently using discontinued parts from Advanced Micro Devices (Sunnyvale, CA), you may be in luck. AMD and Rochester Electronics have entered into an agreement that provides Rochester with all residual products (wafers, dice, finished goods) and access to selected tooling and process "recipes" for discontinued AMD parts. The first products to be transferred are 15 sole-source digital parts.

Rochester also has the right to acquire any additional products that AMD may discontinue in the future. The agreement covers military and commercial sole- and multiple-source products.

Rochester Electronics Inc
10 Malcolm Hoyt Dr
Newburyport, MA 01950
(508) 462-9332
FAX (508) 462-9512

If any other companies are making agreements to manufacture discontinued parts, please fill Ask EDN in on the details. Let's make tracking down obsolete or discontinued parts as painless as possible.

Ask EDN solves nagging design problems and provides answers to difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNPRIME. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.

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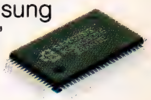
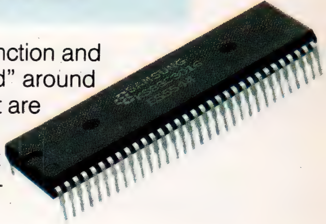
SAM 8 — Innovation in Application-Specific 8-Bit Microcontroller Design

Samsung now offers you the design benefits of product customization with the cost benefits of high-volume, high-yield production techniques. Using the Zilog Super 8® CPU core as a starting point, Samsung has developed modular design libraries or "function blocks" for a wide variety of peripherals, Buses and I/O have been improved and a range of ROM sizes are available.



Introducing the 8-Bit Samsung Arrangeable Microcontroller

To produce SAM8s, application-specific function and memory blocks are selected and "arranged" around the CPU to produce true ASIC devices that are powerful, reliable and affordable. Ask your local Samsung Sales Representative about the SAM8 device that is right for your application.



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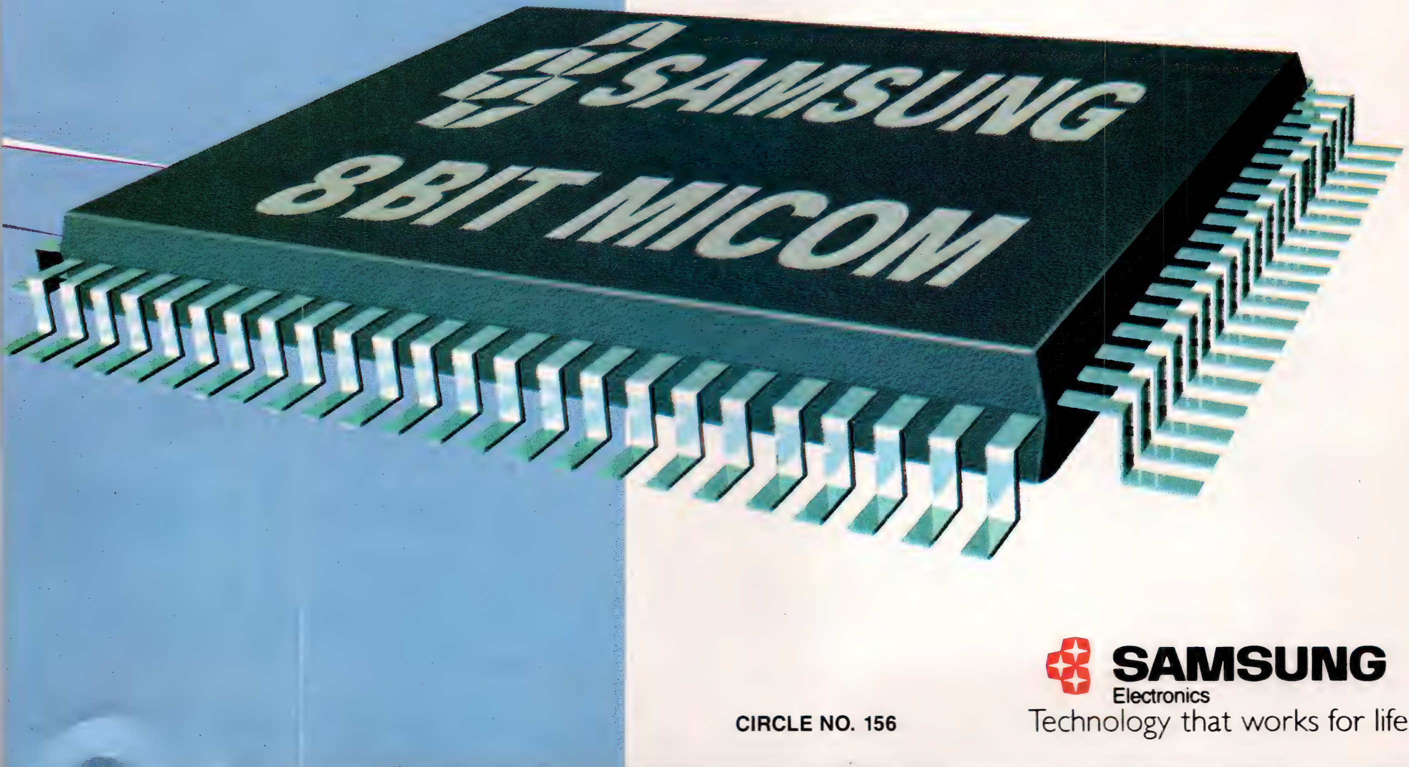
	2K	KS57C0002		KS56C220 KS57C2202					
	4K	KS56C401 KS56C460B	KS57C4004					KS56C450	
	6K						KS56C671*		
	8K	KS57C0108 KS57P0108*		KS56C820 KS56P820* KS56C821	KS57C2408				
	12K						KS56C1270		
	16K	KS56C1660		KS56C1620 KS57C2016 KS57C2616	KS57P2416*	KS56C1610		KS57C5016 KS57P5016*	KS57C3016 (audio dts)
8-BIT	4K	KS88C0504							
	8K	KS88C0016	KS88C0108*						KS88C9108 (IC card)*
	16K		KS88C4116 KS88C0116*						KS88C3016 (TV dts) KS88C8016 (VCR)*
	24K								KS88C3324* (audio dts)
	32K						KS88C7132*		KS88C8032 (VCR)*
	48K								KS88C8148 (VCR)*

*: Under-Development, P: MTP TYPE



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CIRCLE NO. 31

Leave me alone

Now that spring is here, my family and I are thinking about vacation. To me, the best part about vacation is that I'm out of touch with the office for two weeks. Don't get me wrong; I enjoy my work and the people I work with. But when I'm on vacation, they can do without me, and I want to do without them. After two weeks, I'm ready to go back and immerse myself in work—but vacation and work need to be separate.

Today's communications equipment makes it almost impossible to deliberately stay out of touch. But, where I go on vacation, I have no phone, and I'm well away from cellular phone networks. The closest phone is over three miles away at a general store. With direct-satellite communication systems around the corner, I'm not sure how much longer I can hold out. I'm amazed at how much other people like to be in constant communication with home or office. Some people can't live without having a phone nearby.

Of course, there is a time and a place for mobile or portable phones, but, for me, driving to and from work isn't one of them. When I drive to work, I listen to music or a learning tape. Sometimes I drive soundlessly, just thinking about the day ahead or daydreaming. It's pleasant. There's no one I want to talk with, and there's little intelligent I have to say at 6:45 am. On the drive home I often turn on my 2-way radio and find someone to chat with about hobbies, families, jobs, and so on. It's profitless talk, but it's better than getting high blood pressure about a business deal or detail that needs to be worked out at the last minute. I've found that most such communications can wait. I want to leave work behind—at least for a while.

Handy, instant communication is good for business people and others who are on the road a lot. Being accessible and available for suppliers and customers makes a lot of sense. If you spend a lot of your time traveling, a cellular or portable phone becomes a good investment. You can now buy small fax machines that run from a car's battery and attach to your cellular phone. Modem connections are also available. Now as you travel you can get a map, look over a data sheet, or check your electronic mail right from your car. That's making time pay. Recently, I returned a call and was surprised to get a mobile phone's answering system. "I'm sorry I'm not near my carphone right now...," said the voice. I'm not sure whether the answering machine was actually in the car or elsewhere, simply intercepting my call.

Technology is great, and so is communications, but there are times when you need to disconnect yourself from phones and fax machines. I bet your boss, colleagues, workers, and others will survive without you—at least for a few days. So, if you're headed for vacation this summer, try leaving the portable phone at home. If you must take it, remember you can turn it off. Sometimes you just have to say, "Leave me alone."

Jon Titus

Jon Titus
Editor

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.

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Editorial Achievement Awards
1990 Certificate, Best Editorial
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1987, 1981 (2), 1978 (2),
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American Society of
Business Press Editors Award
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Duracell Introdu
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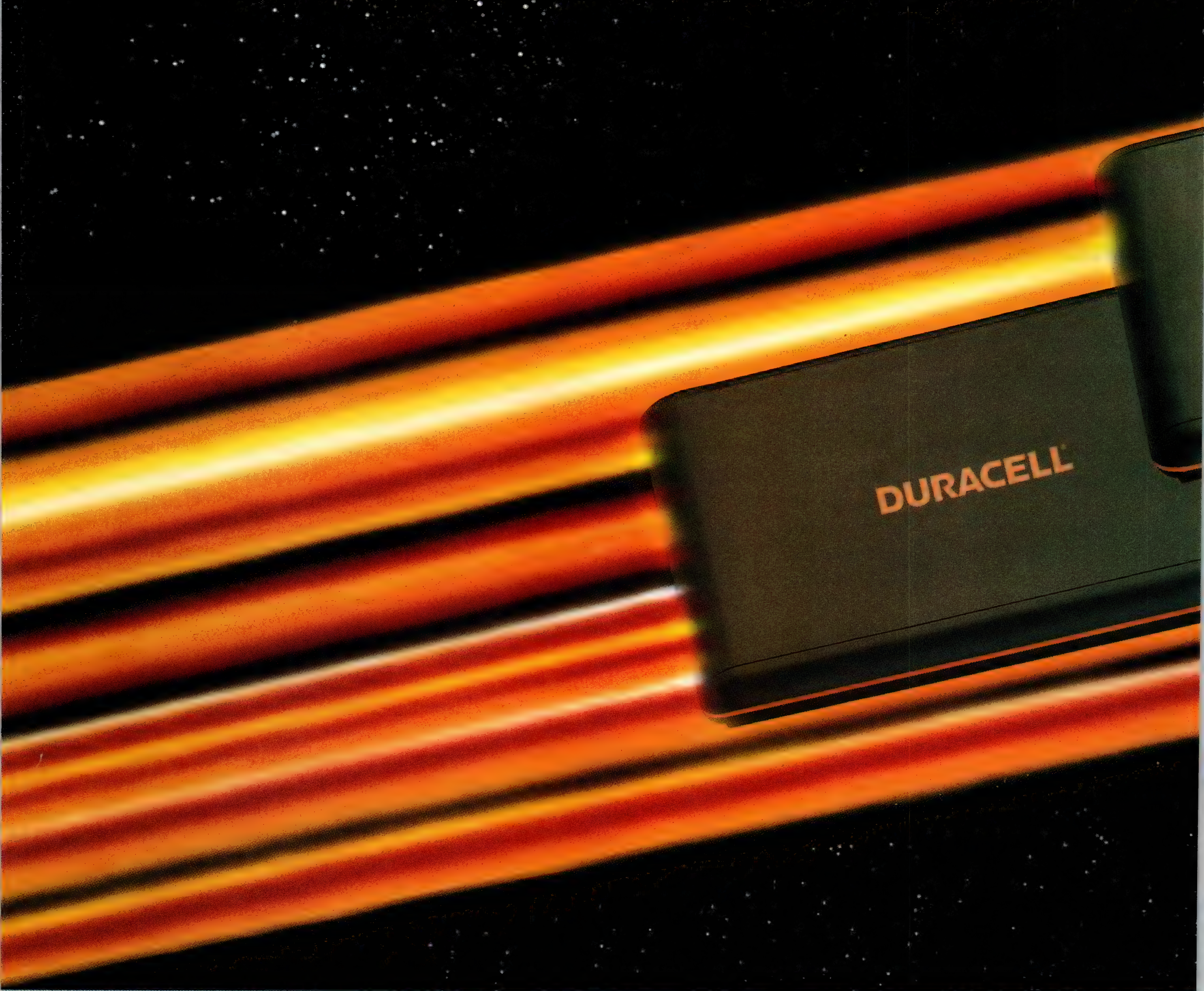

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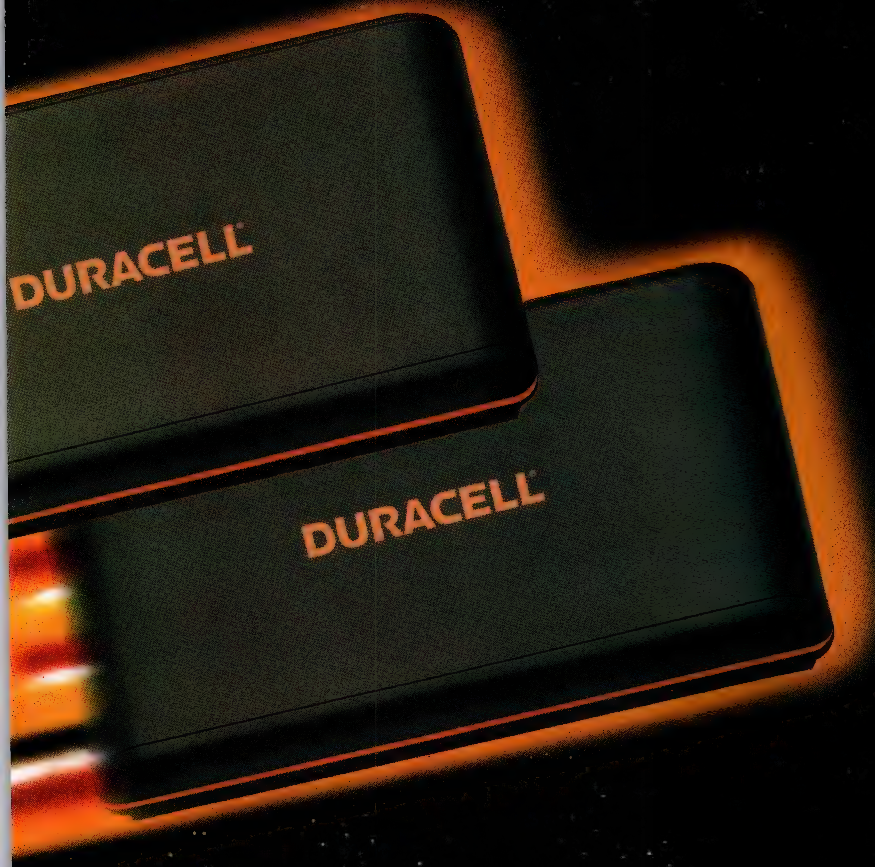

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40-MIPS performance, $0.50/MIPS. TI's 'C5x DSPs can perform an instruction in just 25 ns — for winning 40-MIPS performance at prices as low as $0.50 per MIPS. You can choose from various memory options, up to 10K words of RAM and 16K words of ROM, for even more cost-effective designs. A parallel logic unit (PLU), shadowed CPU registers, block repeats and circular buffers are among the architectural enhancements that enable the 'C5x to boost performance and drive down system costs.

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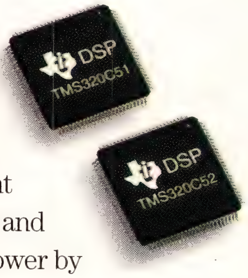

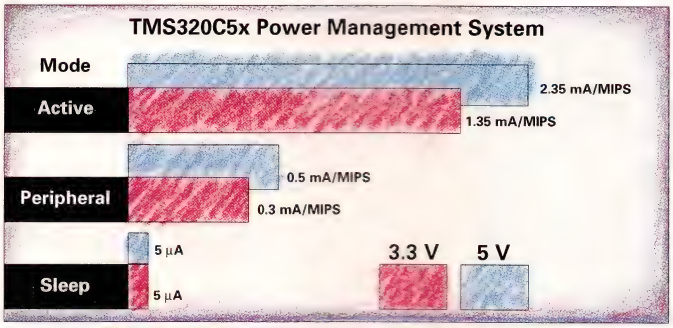

Power management features conserve battery power in today's portable applications.

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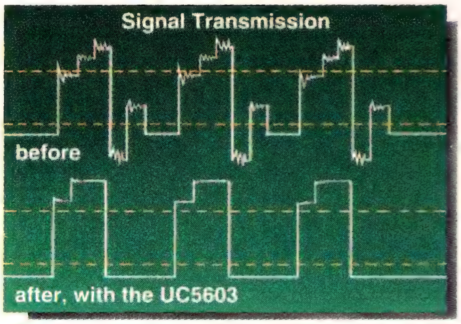

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CIRCLE NO. 33

FPGA design services offer a helping hand

J D MOSLEY, Technical Editor

If you are unfamiliar with FPGAs, designing one on your own may be as inefficient as reinventing the wheel. Turning to an FPGA design expert can cut your development costs and speed your product to market.

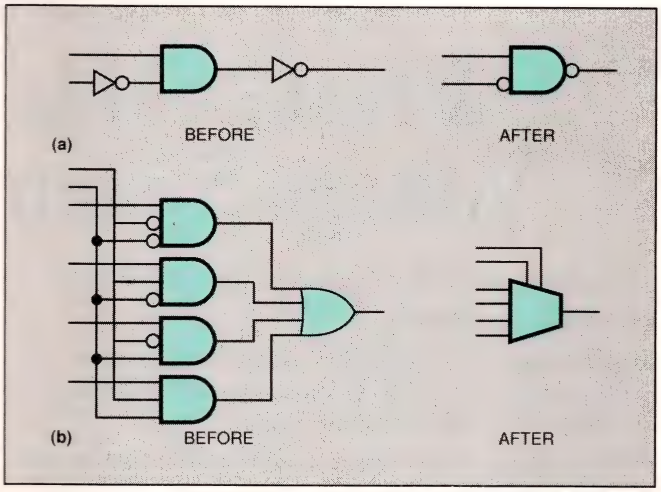
The design flexibility and high-density logic offered by field-programmable gate arrays (FPGAs) let you develop complex, high-speed logic circuits right on your desktop computer. However, the flexibility and high density are precisely what make these devices difficult to program for maximum performance. Although the software tools that help you program FPGAs continue to improve, they remain analogous to paint programs: anyone can use the software, but few can create a masterpiece.

Perhaps the best way to create a FPGA design masterpiece is to call in an independent design expert. If your engineering team is unfamiliar with FPGA tools and techniques, a consultant who specializes in FPGA design can help you avoid the time, expense, errors, and inefficiency that inevitably occur during a learning process.

Some FPGA manufacturers, however, assert that their tools are now so simple to use that even neophytes can easily design FPGAs that perform well. Quicklogic says its newest FPGA software, SpDE Tools Release 3.0, gives novice logic designers the tools to compact logic cells and increase speed. The Microsoft Windows-based software is included in the company's pASIC tool kits, such as the $3995 ECS-Front End (QT-ECS-PC). These kits also provide schematic capture and simulation tools.

Bruce Kleinman, Quicklogic's customer-engineering manager, says the company has tested dozens of customer circuits designed with the tools, from address decoders to 40-bit counters. The test circuits have had up to a 30% boost in speed and up to a 40% reduction in logic-cell use.

Just as design tools vary in their ease of use, so do FPGA architectures. Larry Palley, general manager of Intel's PLD business unit, says that when Intel entered the FPGA market, the company's goal was to make FPGAs as easy to use as small PLDs, with predictability being the payoff for the designer. The company put effort into designing the silicon and the software to make sure that both worked together well. The result has been tools that Palley claims have a 95% success rate.



Bubble pushing (a) and gate collapsing (b) are two optimizing techniques in Quicklogic's FPGA design tools that reduce logic-cell use and boost performance.

Unlike other manufacturers, Intel offers its design tools to its customers free

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Array	Number of Tiles	Number of NPN Devices	Number of PNP Devices	Number of P-JFets	Total Resistor Value-Ohms
2101	4	86	86	0	240K-2.4M
2103	8	158	158	32	480K-4.8M
2104	12	242	242	0	720K-7.2M
2105	16	316	316	64	960K-9.6M
2107	20	390	390	0	1.2M-12.0M

Typical Op Amp Characteristics

- Operating Supply Range: 1.8 volts to 30 volts
- Sleep Mode: Typically 20 microamps
- 2.5 MHz gain bandwidth at 350 microamps
- Output swing within 50 millivolts of supply rail

Sipex

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SIGNAL PROCESSING EXCELLENCE

CIRCLE NO. 34

of charge, and operates a toll-free help line. So, if you try to design the FPGA on your own and run into a snag, you can still call in an expert.

By contrast, design centers typically take a conservative approach unless specifically told to do otherwise, mainly because they want to make sure the design will work. Vacit Arat, director of marketing at Crosspoint Solutions, says design centers will be used more for proof of concept as opposed to getting the last nanosecond out of a design.

Dan LeVasseur, an FPGA consultant with Interface Design, notes that although the devices and tools are improving, you still need the wisdom that comes from experience to fully optimize your device. "Often, the wrong FPGA is chosen for a design. The best qualified consultant would be someone who has designed not only many different applications using FPGAs, but someone who has used many different types of FPGAs, who understands the subtle differences between them, such as gate granularity, product term allocation, and clock distribution. Each of these architectural features is critical in how it relates to a particular application."

Partitioning of a board design is another area where problems can arise. Less experienced FPGA developers may lack an appreciation of the fact that their design is a component of a larger design, and may not understand how their component interacts with the rest of the design. "Perhaps if an entire board can be simulated, including any bus interfaces and FPGAs, then an FPGA expert is not required," LeVasseur says.

FPGA consultants typically charge by the hour because of the uncertainty of most initial designs. However, if the FPGA is part of a complete board design, you may be able to negotiate a fixed price. For your money, you'll get the expert's design notes, flow charts, high-level descriptions, functional descriptions, and object and source files.

Manufacturers offer expertise

No one understands an FPGA better than the manufacturer. So when Mentor Graphics established its six ASIC design centers, Xilinx agreed to participate. These top-down design centers offer an integrated design-flow environment that promotes design predictability for Xilinx XC2000, XC3000, and XC4000 FPGAs. The centers are located in San Jose, Denver, Boston, Dallas, Munich, and Tokyo.

Dan Ganousis, manager of Mentor Graphics' ASIC design centers, says that if you've never used synthesis tools or hardware description languages, you need an expert. He adds that most customers either are interested in replacing ASICs with FPGAs, or they want to use FPGAs for computer-aided prototyping and design verification.

"About two-thirds of what we do is on-site consulting, typically for two to four weeks. When people are starting a new project, we help them. We bring in the experience to save them from having problems later on. Some customers are quite willing the first time through to hand it over, but they still manage the projects," Ganousis says.

He points out that third-party consultants generally assist companies with small design teams that sell in low-volume/high-margin niche markets. These companies use FPGAs as a production device in their final product. In contrast, larger companies are attracted to FPGAs as prototyping tools for

FPGA design experts want to hold your hand

You don't have to suffer through an FPGA design problem alone. Even proficient logic designers may need a helping hand from time to time. Rather than jeopardize your circuit's timing efficiency or prolong your product's time-to-market, maybe you should swallow your engineering pride and delegate at least some of the design details to an independent expert.

Some benefits of FPGA design services are:

- Meeting speed and timing requirements
- Meeting production deadlines
- Initiating novices to the intricacies of FPGA design
- Smoothing an experienced designer's transition from PLDs to FPGAs
- Selecting and introducing the use of timing-driven synthesis tools and equations
- Shortening the learning curve when a designer switches to a new FPGA architecture
- Decreasing the capital investment necessary to adopt a different FPGA architecture
- Providing insight into efficient logic design
- Helping a design team select the best logic architecture for a specific project
- Fine-tuning effective logic mapping, placing, and routing
- Assisting in the development of timing constraints and specifications
- Interpreting FPGA data sheets to extract logic-propagation and interconnect-delay information
- Prioritizing the routing of logic nets and reducing interconnect delays by shortening propagation paths
- Altering logic design to maximize speed and minimize slack time by means of timing analysis
- Minimizing the ease with which competitors can reverse engineer your design.

proof-of-concept verification and concurrent software development.

Prototypers prefer to use reprogrammable static-RAM-based FPGAs, such as those that Xilinx manufactures, so they can correct functional errors in the logic as they discover them. However, the overhead in tools and equipment is higher for these FPGAs than for antifuse FPGAs, such as one-time programmable Actel devices. Short- to medium-volume manufacturers prefer antifuse devices due to their low cost and nonvolatility.

Andy Haines, Actel's director of marketing, says antifuse FPGAs help meet time-to-market needs by enabling rapid customization and product differentiation without the up-front development charges associated with ASICs. In this way, companies minimize the time and money spent on inventory and reduce the risk of getting stuck with obsolete devices. The nonvolatility of antifuse FPGAs makes them very stable and reliable, and the simplicity of the devices translates into consistent ease-of-use.

LeVasseur notes that, "A person who has the invaluable experience of going through similar FPGA design cycles in the past has an edge over someone who has not, no matter how easy the tools are to use. Using a consultant will also increase the odds that a design will not have to be 'respun,' causing expensive schedule slips and other costs."

However, as Arat observes, you definitely give up some degree of control when you hire an FPGA consultant. He notes that the more changes there are to your design, the harder it may be to manage. Companies often overlook the management overhead. His advice for companies seeking outside design assistance is to "develop a relationship and stick with it."

In short, don't expect to dump your design on an FPGA design expert and come back in a couple of weeks to pick up the perfected results. To get the best possible design for your project, you have to work closely with your expert. Think of him or her as another member of your design team who will require as much guidance regarding the goals and requirements of the project as any other newly assigned engineer.

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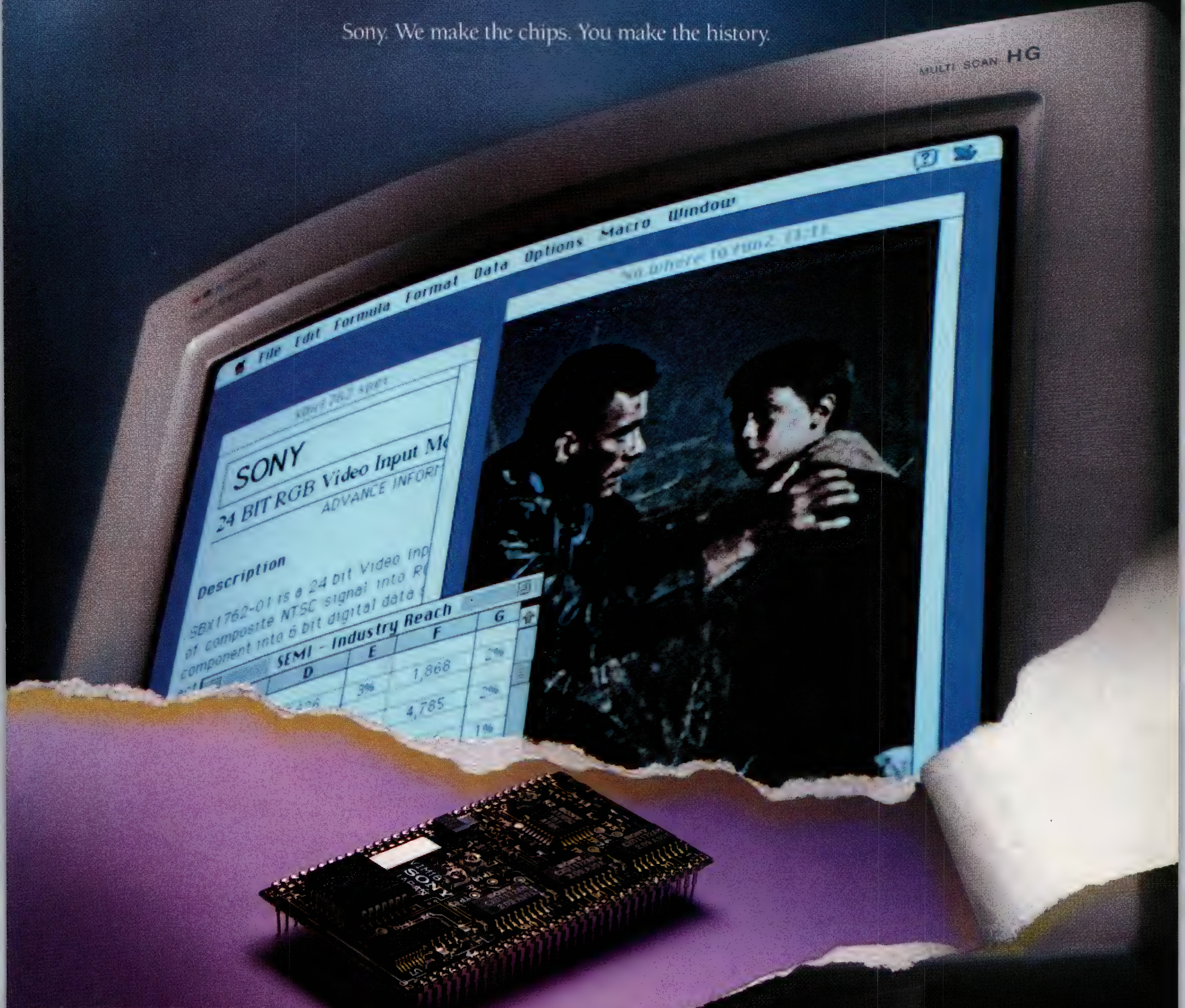
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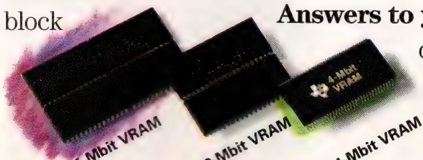

VRAM COMPARISON

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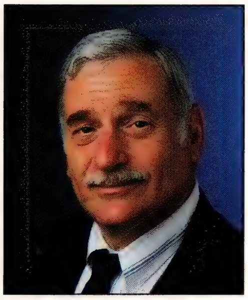
Design low-cost, quick-and-dirty applications with 8-bit μCs

RAY WEISS, Technical Editor



The world of low-cost, down-in-the-dirt microcontroller (μC) applications is booming. Eight-bit μCs are tackling everything from car keys to alarm systems to personal electronics, and are invading the traditional commercial turf of 4-bit μCs. Today's designers run with minimal μCs and spin out products in development cycles unheard of five years ago.

In this hard and fast world, cost is everything. "We all beat up on the chip vendors to get the costs down," says Doug Deeds, a project engineer at TE Electronics (Fort Worth, TX), formerly Tandy Electronics. "And then we live within tight cost constraints." Engineers scramble to cut costs by finding the cheapest μC suitable for the job and by minimizing power, real estate, and support chips.

Many engineers thrive in this environment. "I like solving problems," says Deeds, "it's a challenge to bring in solutions at a low cost." And unlike larger projects, many of these low-end jobs are one-man tasks. "The nice thing at the low end is that one guy, you, gets to do all the software and maybe all the hardware design, too," says Paul Hoseit, analog group manager at C&K Systems (Fulsome, CA), a vendor of alarm systems.

Many design shops use whatever μC family gives them an advantage. "We've looked at and worked with most low-end μCs, looking for the right combination of peripherals and price," says Deeds. "Our needs are specialized, and it's hard to find the right peripherals without having to pay for a lot of unwanted peripherals and unused silicon."

Not all 8-bit μCs can compete in this low-end derby. Cost is the driving factor, and silicon ain't cheap. Chip vendors continually juggle their limited silicon budgets to find the "silicon sweet spot"—that magic combination of processor throughput, μC resources, peripherals, and cost. Winning μCs combine minimal pinouts, small RAM and ROM capacities, low power, and few peripherals. Such families include

Cost is everything when you're designing low-end, 8-bit-μC applications. You've got to find the cheapest μC for the job, minimize power and real estate, and use as few support chips as possible.

- **Motorola's 68HC05.** Descended from the classic 6800, the 05 is an accumulator-based architecture with a clean instruction set. A minimal implementation, the family's chips include a simple timer, a watchdog timer, and an optional small EEPROM. The 68HC05 family has over 130 variations and leads 8-bit-μCs in sales. The new 68HC05Kx is a minimal 05 and has a simple timer, a watch-dog timer, 32 bytes of RAM, and 504 bytes of ROM.
- **Intel's 80C51.** This chip isn't exactly a low-end μC, but it fits into the lineup because you can get one for less than \$2.50. In fact, the 8051 is second in the μC sales derby, right behind the 68HC05. Intel developed the 8051, but there are several second sources and a wide range of variations. One licensee, Philips, added an I^2C 2-wire serial bus, which links μCs and peripherals.

- **Philips-Signetics's 80C751/752.** Philips engineers squeezed the 8051/52 design into a 24-pin 300-mil DIP for tight designs. The 751/752 integrates 8051 power with reduced real estate and an on-chip I^2C bus.
- **National Semiconductor's COP8.** A pioneering 8-bit chip, the COP8 is low-cost and accumulator-based; some parts cost less than $1 in volume. COP8s include the Microwire 3-wire serial commu-nications bus, which links proces-sors and peripherals. National also sells peripheral and memory chips that interface to the Microwire bus. Some COP8s have brownout pro-tection, analog comparators, or LED drivers.
- **Microchip Technologies' PIC 16C5x.** PIC µCs combine a simple instruction set, fast 200-nsec execution, and minimal peripherals. The low-end 16C5x chips lack interrupts and multiply and divide instructions. But PIC µCs' speed, low pin counts, and static design make them a good choice for a wide range of low-end applications.
- **SGS-Thomson's ST6.** The ST6 is a minimal, accumulator-based design. It's a slower, serial implementation but includes an 8-bit ADC, a watchdog timer, and a simple timer. The ST6 has a simple instruction set and a 6-level hardware stack. Like the PIC µCs, it lacks multiply and divide instructions. Low-end versions come in a 20- or 28-pin package.
- **Texas Instruments' TMS370.** This µC is a slow but sophisticated chip. Peripherals in-clude a serial peripheral interface (SPI), 24-bit watchdog timer, 16-bit configurable timer, and EEPROM. Low-end versions come in a 28-pin package.
- **Zilog's Z8.** The Z8 is a compact chip that has several variants. Peripherals include an SPI, brownout-protection hardware, watchdog timer, analog comparators, and two 8-bit counter/timers—all in packages having as few as 18 pins. The Z8 µC uses 144 8-bit registers arranged in 8-register banks. Larger register files are also available.

Most of these chips have power-saving modes, and many work at voltages as low as 2.0V. Additionally, some µCs are static designs, which lets you trade lower clock rates for lower power dissipation. For example, in a car transmitter application, United Technologies' (Dearborn, MI) Senior Engineer Gerald Brehmer runs a Microchip PIC 16C5x at 32 kHz. "It really makes the batteries last," he says, "and lets me use a cheaper crystal."

Down-in-the-dirt µC applications include security peripherals, alarm systems, and automotive controls. Most of these systems must live in 0.5 to 4 kbytes of ROM and run in 32 to 256 bytes of RAM. "It's a real battle fitting code into ROM," says Howard Hasehuhn, a project engineer at Donnelly Corp (Holland,

Table 1—Representative low-end 8-bit µCs

Vendor, chip	Clock (MHz)	Base instruction cycle	I/O pins	Package	Memory	Voltage ranges	Timers
Intel 80C51 Circle No. 378	12	12-clock cycle 1-µsec ADD/NOP	32	40-pin DIP 44-pin PLCC	128 bytes RAM 4 kbytes ROM	5V	2 16-bit timers
Microchip PIC 16C54 Circle No. 379	20 (static)	200 nsec (pipelined) 400 nsec (branch)	12	18-pin DIP 18-pin SOIC	32 bytes RAM 512x12 bits ROM	3.0 to 5.5V	1 8-bit timer
Motorola 68HC05K1	4, 2 internal	1-µsec ADD/NOP	10	16-pin PDIP 16-pin SOIC	32 bytes RAM 504 bytes ROM 8 bytes OTP/ personality EPROM	3.3 to 5.5V	1 15-step timer
68HC05J1 Circle No. 380	4, 2 internal	1-µsec ADD/NOP	14	20-pin PDIP 20-pin SOIC	64 bytes RAM 1 kbyte ROM/ EPROM/OTP	3.3 to 5.5V	1 15-step timer
National Semiconductor COP820CJ Circle No. 381	10 (static)	2-µsec ADD/NOP	12	16-pin SOIC 20-pin DIP	64 bytes RAM 1 kbyte ROM	2.5 to 6.0V	1 16-bit timer (with capture or autoreload)
Philips 80C751 Circle No. 382	12	12-clock cycle 1µsec ADD/NOP	19	24-pin DIP 28-pin PLCC	128 bytes RAM 4 kbytes ROM	5V	1 16-bit timer (with capture or autoreload)
SGS-Thomson ST6210 Circle No. 383	8	6.50-µsec ADD/LOAD	12	20-pin PDIP 20-pin SOIC	64 bytes RAM 2 kbytes ROM	3.0 to 6.0V	1 8-bit timer
Texas Instruments TMS370C311 Circle No. 384	5	1.6-µsec ADD/NOP	22	28-pin DIP 28-pin PLCC	128 bytes RAM 2 kbytes ROM	5V	1 16-bit timer with 1 compare reg and 2 capture regs
Zilog Z86L06 Circle No. 385	8	1-µsec ADD/NOP	14	18-pin DIP 18-pin SOIC	128 bytes RAM 2 kbytes ROM	2.0 to 6.0V	2 8-bit timers

MI), a supplier of automobile motor-controlled mirrors. "ROM is the problem. You can work around RAM limitations by designing code to use ROM instead, or by not keeping stuff in registers and paging working registers."

Hoseit, of C&K Systems agrees, "The hardest thing is fitting code into ROM, especially as project requirements continue to change. That's why it's nice to work with a family of µCs—if you have to, you can move up to a larger ROM size without a redesign."

One way manufacturers reduce µC costs is by reducing chip pinouts. In general, pin counts for low-end, 8-bit µCs range from Motorola's 16-pin 68HC05K to TI's 28-pin TMS370C01x.

Low-end µCs usually have 12 to 22 I/O pins. If you have to drive a lot of logic, having few I/O pins can make life difficult by forcing you to use a multiplexer for more signal lines. Fortunately, some applications don't need more than a few I/O signals. "For our applications, we don't need a lot of I/O pins," says John Sherman, a senior engineer at Supra Products (Salem, OR), an alarm manufacturer. "We use serial EEPROM to hold data and serial ports to move data."

As Sherman notes, serial EEPROM reduces large µC pinouts. You can read or write data serially to an EEPROM using one or two lines, rather than using an 8-bit port and adding extra logic to multiplex addresses and data.

One interesting trend is a move toward one-time-programmable (OTP) memory-based processors. "One of our requirements for a µC is that it have an OTP version," says United Technologies' Brehmer. "We need OTP memory for internal prototypes, and our customers like to get prototyping parts early in their design cycle." OTP parts still cost more, so many engineers are reluctant to use them for final production. But many use OTP µCs for initial product runs and fast revisions and to minimize part stocks.

Another trend is the increasing use of nonvolatile memory, both EPROM and EEPROM. Many applications, such as security, need an on-chip mechanism for encoding part-specific data. On-chip EEPROM lets µCs retrieve and hold key information in the field. However, EEPROM uses more silicon than other memories, tends to have longer write cycles (typically 10 msec), and has a lifetime write limit on the order of 100,000.

Designing low-end 8-bit systems is definitely not like flying first class. When pennies count, you must forgo the peripherals many engineers take for granted.

Most low-end applications don't need a lot of timing functions. Many deal with only one or two time events, which is good news because low-end µCs have pretty simple timers. You can program the COP8's timer to act as a pulse accumulator, a timer with a capture register, or a timer with a compare register. The Z8 has two 8-bit timers, and the 8051 has two 16-bit timers. The TMS370C010's one 16-bit timer is positively luxurious—it has one input capture and two compare registers. Philips's 80C751 has one 16-bit timer with an autoreload feature.

Many applications don't need an ADC because they deal mainly with digital signals, and many analog signals can be converted using RC networks. However, if you have analog inputs, an ADC can save you some external circuitry. The ST6 has an ADC. Others, including the COP8 and Z8, have one or more analog comparators for coarse signal conversions. These µCs are adequate for applications that use fairly gross analog measurements for temperature or movement.

Low pin counts limit the number of external interrupts, and most

Safety features	External interrupts	Other features/comments	Price (10,000)
—	2	I²C serial bus	Less than $2.50 from Intel and second sources
Watchdog timer with RC clock	0	33 instructions, accumulator-based 2-level stack	$0.80 (100,000); $1.25, OTP version
Watchdog timer	1	Low-end 68HC05, 4-keyboard scan	$0.75 (50,000); $1.93, OTP version
—	1	Low-end 68HC05	$0.97 (50,000)
Watchdog timer, brownout detection	3	2 analog comparators	$1.27
—	2	I²C serial bus	$1.95
Watchdog timer	1	31 instructions 6-level stack 8-bit ADC	$1.96
Watchdog timer	3	Serial peripheral interface	$1.50 (25,000)
Watchdog timer, brownout detection	1	2 analog comparators	$1.45

low-end μCs make do with one. A single interrupt line may force you to add additional logic to multiplex interrupts. Alternatively, you could use periodic polling to check inputs for hardware events. Exceptions are the TMS370Cx1x, which has three external interrupts, and the 68HC05K1, which has four keypad-input interrupt lines and one external interrupt line.

On the positive side, these 8-bit μCs do have some useful peripherals. Many low-end μCs have serial interfaces such as UARTs, SPIs, Microwire bus, and I²C bus. These serial interfaces let you move data serially with a minimum of bit-banging. Even better, the Microwire and I²C buses are full serial-bus protocols that support multimaster operation and access to peripheral chips. "I use the Microwire serial bus to connect μCs to chips such as serial EEPROMs," says Donnelly's Hasehuhn. "You don't need any decode logic; it's built into the chips."

The I²C bus has an additional advantage: It's the base for the emerging Access subsystem bus standard. Several system companies use the Access bus to easily link in slow desktop peripherals such as keyboards, mice, scanners, and light pens. A product built on an I²C bus can easily interface to Access bus systems.

Supra's Sherman used both the I²C and Multiwire serial buses to link an 8051 to a COP8 in a real-estate lock-box application. The control card—or key—holds the 8051, batteries, and data in EEPROM; the lock box has a COP8 to control the lock. The CPUs communicate via the mixed serial buses.

Another peripheral—and safety feature—you'll find on many low-end μCs is a watchdog timer. A watchdog timer helps ensure that your code sticks to business and doesn't lock up into an indeterminate loop.

"If your PC locks up, you can just power off and restart," notes Tim Roddy, electronics design manager at United Technologies. "But when it comes to things like cars, you can't just go out and disconnect the car's power cables when a μC locks up. Instead, we need to build in reliability and fail-safe operations to meet stringent safety requirements. Moreover, it's not enough to make sure code works, we also need to know what breaks it and what it will do under those conditions."

Watchdog timers are a "catch-yourself" monitor: You set a count-up or -down value, and if the watchdog is not periodically reloaded before bottoming out, it stops processing. If your code locks up, the theory goes, the watchdog will time out and sound the warning. Often, a watchdog timeout triggers a CPU reset or nonmaskable interrupt. Low-end μCs with watchdog timers include the COP8, PIC 16C5x, 68HC05, TMS370, ST6, and Z8.

Another safety feature is brownout detection. Special hardware detects when power drops below a specific level and interrupts the system. Typically, a brownout condition triggers a power-on interrupt, which passes control to the power-on sequence. Brownout detection is important for many control applications because the microprocessor's state and execution can be indeterminate at unrated power levels, which can lead to application damage. Low-end μCs with brownout detection include the Z86L06 and COP820CJ. EDN

Acknowledgment

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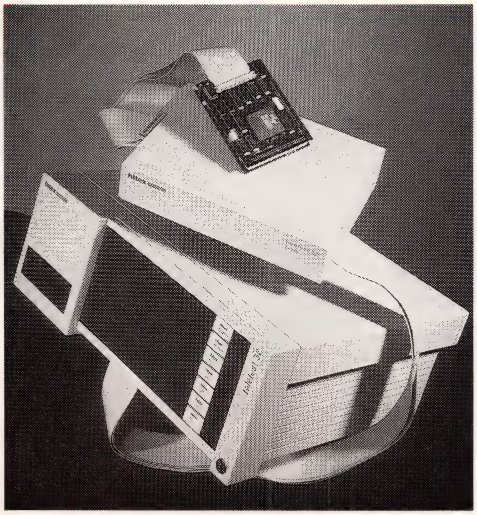

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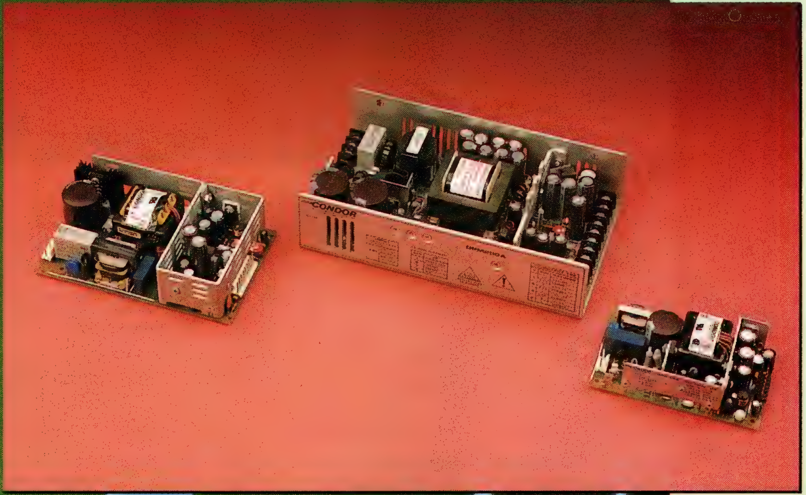

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CIRCLE NO. 42

Flash-memory ICs redefine program and data storage for portable applications

GARY LEGG, Senior Technical Editor

A single flash-memory chip can provide nonvolatile, updateable storage for execute-in-place program code. Multiple chips can create solid-state mass-storage systems.

New architectures for flash-memory ICs are making it possible to implement solid-state mass storage and modifiable, execute-in-place program storage. Together with a trend toward lower voltages, the new architectures are making flash a key technology for small, portable computers and other items, such as cellular phones.

Block-erase capability is common to all the new architectures. In contrast to first-generation flash, which could only be reprogrammed by erasing and rewriting an entire IC, second-generation flash can be reprogrammed a block at a time. Block sizes range from 64 bytes to 64 kbytes, depending on the chips' intended applications.

Many new flash chips target either mass storage or program storage as a primary application (**Table 1**). Mass-storage architectures stress convenient memory updating and, in some cases, disk emulation. Program-storage architectures (**Fig 1**) divide programs or system code, such as a PC's basic I/O sys-

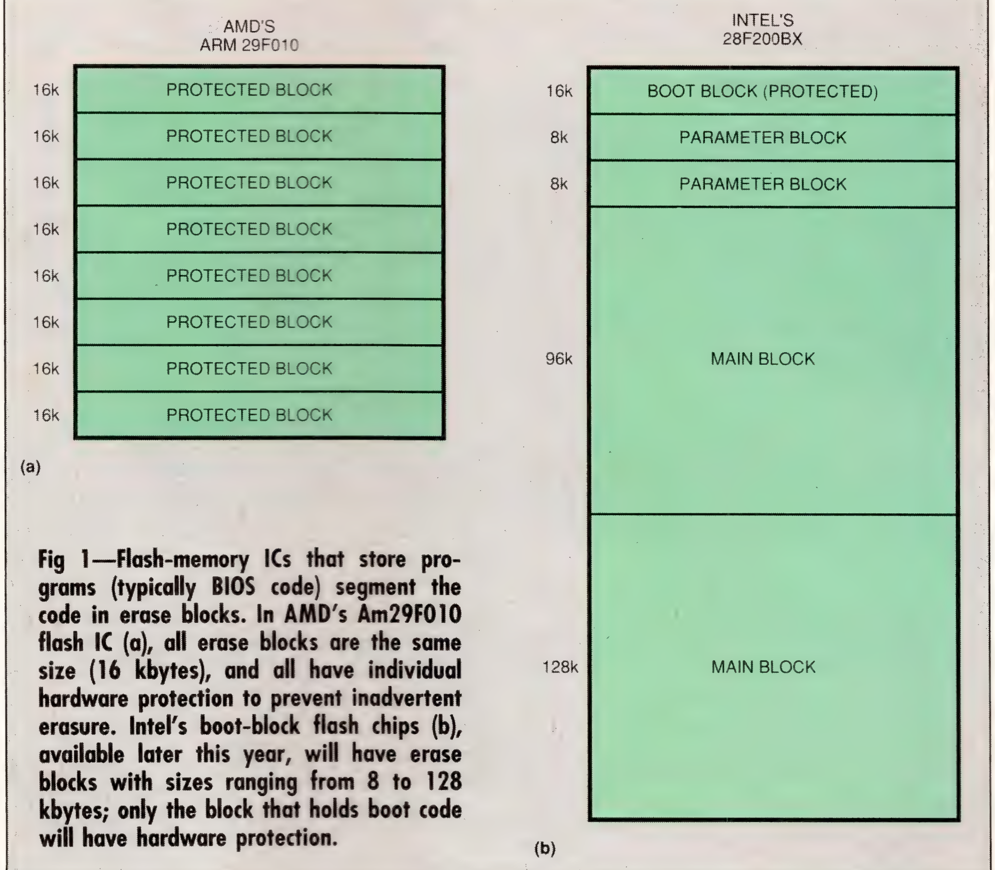

Fig 1—Flash-memory ICs that store programs (typically BIOS code) segment the code in erase blocks. In AMD's Am29F010 flash IC (a), all erase blocks are the same size (16 kbytes), and all have individual hardware protection to prevent inadvertent erasure. Intel's boot-block flash chips (b), available later this year, will have erase blocks with sizes ranging from 8 to 128 kbytes; only the block that holds boot code will have hardware protection.

tem (BIOS), into segments. Some of the segments are easy to update, and others—for critical code—are hardware protected.

Most of the second-generation flash ICs are forsaking dual-voltage operation for a single voltage. Although chips from market-leader Intel still require a separate 12V source for erasing and writing, new and upcoming flash ICs from Advanced Micro Devices (AMD), Atmel, and Toshiba read, erase, and write with a single 5V supply. Some of the new architectures are just now becoming available in ICs; others will be ready at various times during the year.

Most flash vendors also have 3.3V products in development; Atmel, in fact, is already delivering some. Intel plans to use 3.3V for reading but will stick to 12V for erasing and writing. Other manufacturers plan 3.3V-only ICs.

Potentially low costs are adding to flash's appeal. Flash technology requires only one transistor per memory cell, making flash ICs very dense and thus potentially cheap to produce. According to some estimates, flash memory will cost less than DRAM within the next two or three years.

For now, though, difficult manufacturing processes are keeping flash prices high and production low. Prices per megabit of capacity range from around $4 to $25 and higher, depending on a chip's architecture, capacity, and performance. Only a few companies are selling flash in volume, although the number of manufacturers is increasing.

Looking like EEPROM

In many ways, flash is starting to look like the EEPROM technology that it was intended to compete with. Not only do some chips erase and write with the same 5V used for reading, but a few actually use EEPROM's physical processes for reprogramming. In essence, many flash chips are EEPROMs without byte-level alterability.

Block-erase capability is an intermediate approach between EEPROM's byte erase and first-generation flash's bulk (whole-chip) erase. Atmel's flash ICs, based on EEPROM technology, have erase blocks as small as 64 bytes; chips from other vendors have blocks that range from 4 kbytes (Toshiba) to 64 kbytes (Intel). First-generation, bulk-erase chips are available from AMD, Catalyst, Fujitsu, Hitachi, Intel, Mitsubishi, and Texas Instruments. Even some of these first-generation devices are just now entering production, however.

In mass-storage applications, block-erase capability allows flash-resident files to be updated piecemeal, rather than being entirely replaced. Indeed, some flash manufacturers refer to erase blocks as erase sectors—as in disk sectors.

The erase blocks of some flash ICs even match disk sectors' 512-byte size. For example, Sundisk (Santa Clara, CA), Silicon Storage Technology ((SST), Sunnyvale, CA), and Oki Semiconductor all make PCMCIA flash-memory cards using flash chips that have 512-byte

Table 1—Flash-memory ICs

Manufacturer	IC designation	Capacity (bits)	Voltages (read/program)	Erase-block size (bytes)	Availability	Primary application	
						Mass Storage	Program Storage
AMD **Circle No. 351**	Am29F family	1M	5/5	16k	Now	x	x
		4M	5/5	16k	This year	x	x
Atmel **Circle No. 352**	AT29 family	256k	5/5, 3.3/3.3	64	Now		x
		512k	5/5, 3.3/3.3	128	Now		x
		1M	5/5, 3.3/3.3	128	Now		x
		4M	5/5, 3.3/3.3	512	This Year		x
Hitachi **Circle No. 355**	HN28F4001	4M	5/12	16k	This year	x	
Intel **Circle No. 356**	28FxxxBX (Boot block)	2M	5/12	8k to 128k	This year		x
		4M	5/12	8k to 128k	This year		x
	28F008SA (Flash file)	8M	5/12	64k	This year	x	
Toshiba **Circle No. 360**	TC58 family (NAND)	4M	5/5	4k	Now	x	
		16M	5/5	4k	Now	x	

Note: Prices for flash-memory ICs vary greatly, depending on architecture, capacity, performance parameters, and quantity purchased. Contact manufacturers for details, but expect to pay $4 to $25 per Mbit of capacity.

For more information . . .

For more information on the flash-memory products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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sectors (**Ref 1**). Of the three companies, however, only Oki plans to make ICs available to customers.

Flash ICs designed for mass storage emphasize either fast writing or fast reading. Small erase blocks allow frequent, fast file updates, because fewer memory locations have to be changed; the chips on memory boards from Sundisk and SST and the ICs from Oki take this approach. Toshiba's chips, on the other hand, reduce the erase and write times per byte. Intel and AMD, noting that most application programs read far more often than they write, emphasize read speed for their flash products.

Comments
Individual hardware protection on all erase blocks. Read access 55 nsec now, 45 nsec soon. Negative-gate erasing reduces power consumption.
EEPROM technology. Some available with 90-nsec read access.
EEPROM technology.
Hardware protection on 16-kbyte boot block. Read access 60 nsec, 80 nsec. 3.3V versions in development.
Read access 85 to 120 nsec. 3.3V versions in development.
NAND-gate cells differ from conventional NOR-gate cells. Slow random access (15 μsec); moderate average access (140 to 150 nsec/byte). Page programming: 512-byte pages for 4M device, 256-byte pages for 16M device. Fast programming averages 350 nsec/byte.

For program-storage applications, fast reading is essential; otherwise, a flash-resident execute-in-place (XIP) program will slow down the processor that it runs on. Access times around 60 nsec will allow 16-bit microcontrollers for embedded control to run with no wait states. AMD chips beat that time, at 55 nsec, and soon will reach 45 nsec. Intel's second-generation program-storage chips, when available later this year, will have access times of 60 and 80 nsec.

Erase blocks in program-storage flash chips allow piecemeal updating of system code or application programs. System BIOS can require frequent updating, because software companies are adding new features to take advantage of new technologies. Two recent additions are power-management capabilities and software services for PCMCIA cards. To accommodate such additions, program-storage flash chips are gaining capacity—to as much as 4 Mbits.

Protection from viruses

To protect critical code from unwanted alteration, as from computer viruses, program-storage flash chips provide hardware protection for one or more erase blocks. It's possible to change the code in a protected block, but unauthorized changes are difficult. Intel boot-block ICs protect one block, which holds boot-up code; AMD's second-generation flash chips have individual protection for all blocks.

Erase blocks in program-storage flash chips can all be the same size or have different sizes. Each approach has its merits.

The blocks in AMD's Am29F family of ICs are a uniform 16 kbytes, a size that AMD claims provides versatility for a variety of applications. AMD promotes its latest flash products as being suitable for mass

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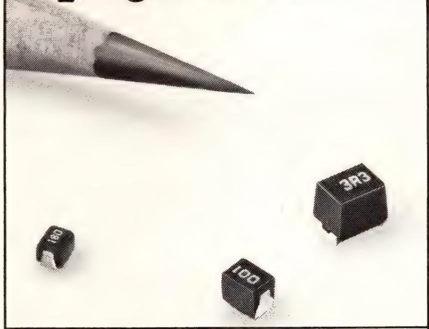

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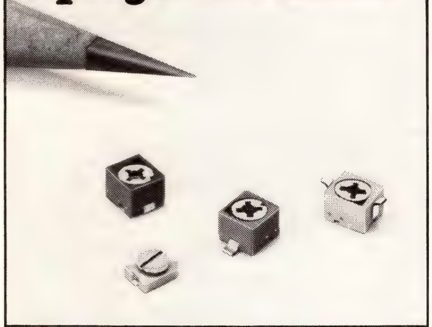

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FLASH MEMORY

storage as well as program storage.

Intel's boot-block chips, on the other hand, are aimed solely at program storage; 8-kbyte blocks hold program parameters, a 16-kbyte block holds boot code, and much larger blocks (96 and 128 kbytes) hold program code.

Choices in voltages

Ultimately, differences in voltage requirements may affect design choices more than differences in architectures. First-generation flash ICs use both 5 and 12V; virtually all second-generation products except Intel's require only 5 or 3.3V.

The choice between single-voltage and dual-voltage flash boils down to design elegance versus cost. Single-voltage flash eliminates the need to include a 12V programming circuit in a system design, but it does so by putting a charge pump in each chip. Because systems usually update only one chip at a time, a better approach, according to Intel, would be to put a single 5-to-12V converter in your system. The total cost of parts for the converter would be about $4. Other companies counter that single-voltage flash chips save power, make system design easier, and save the space and weight of a converter.

Changes in flash technology are making it possible for on-chip charge pumps to get smaller (and thus cheaper) and also reduce power consumption. The use of EEPROM-type technology for flash is one such change; new erasing and writing schemes in conventional flash are another.

The single-voltage flash chips that use EEPROM technology perform both erase and write functions with Fowler-Nordheim tunneling, which requires less power than the hot-electron processes of conventional flash (**Ref 2**). Atmel's and Toshiba's chips are examples of EEPROM-type flash.

AMD's single-voltage chips are "true" flash, but they reduce power consumption and the size of charge pumps by using a novel approach for erasing and writing. AMD's negative-gate erase scheme uses a small charge pump to apply −10.5V to the gate of a memory cell's transistor while applying 5V to the transistor's source. The charge pump needs to deliver less than 10 μA of current at −10.5V, while the main erase current at 5V is between 10 and 20 mA. By comparison, conventional erase schemes apply 12V to the transistor's source and deliver 10 to 20 mA of current.

Low-voltage flash is coming

Whether or not single-voltage flash continues to proliferate, the use of 3.3V for reading most certainly will. Portable systems demand low voltage, and shrinking chip geometries require it for reliable operation. Shrinking chip geometries increase flash ICs' storage capacities, too. Within a year, several companies expect to have 16-Mbit chips.

From the second generation of flash that is just now appearing, designers will choose which architectures succeed and which do not. When those choices are clear, and when flash manufacturers solve their production problems, then prices will fall. And then, with flash chips' storage capacities increasing, a flash revolution could be underway. EDN

References

1. Legg, Gary, "Flash memory challenges disk drives," *EDN*, February 18, 1993, pg 98.
2. Gallant, John, "Conventional EEPROMs and flash EEPROMs offer a spectrum of bit densities," *EDN*, October 27, 1988, pg 89.

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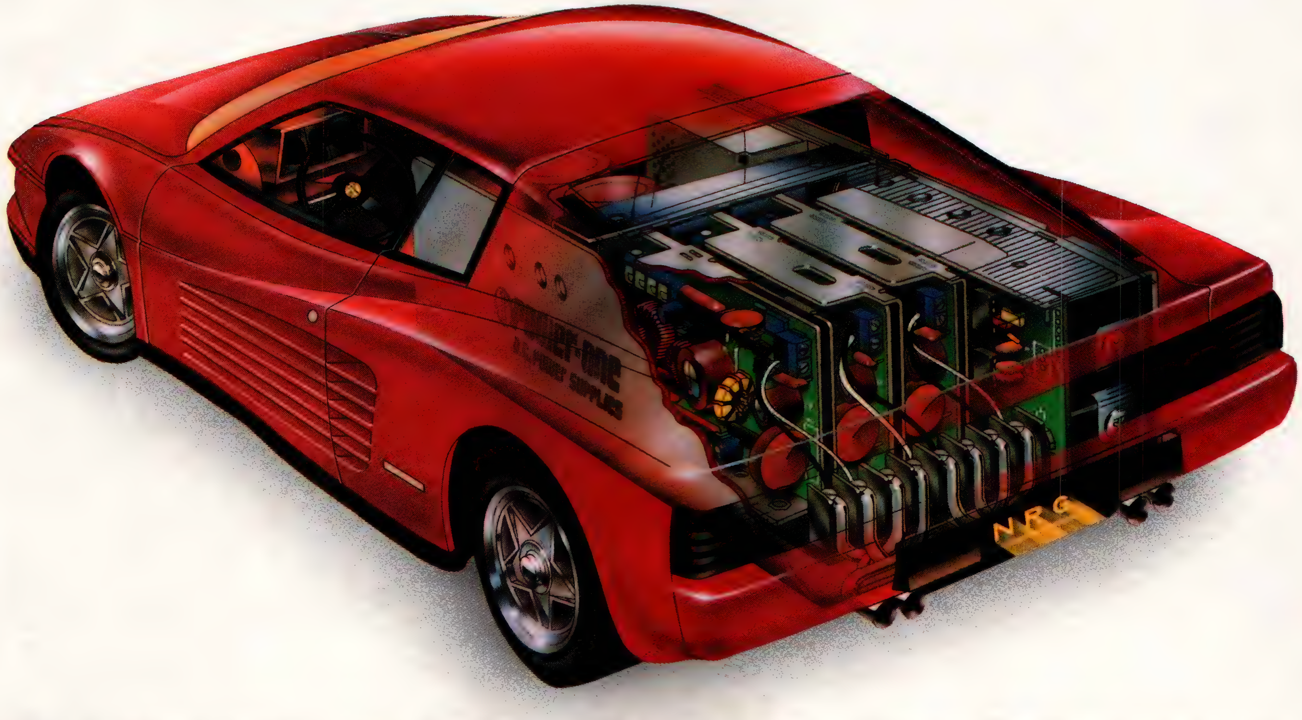

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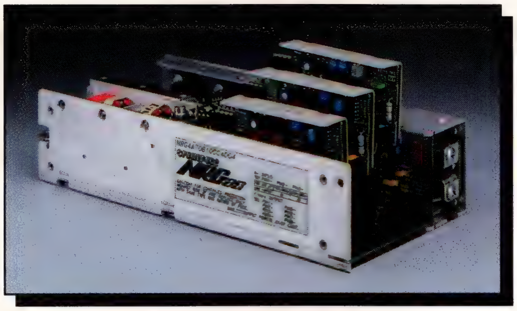

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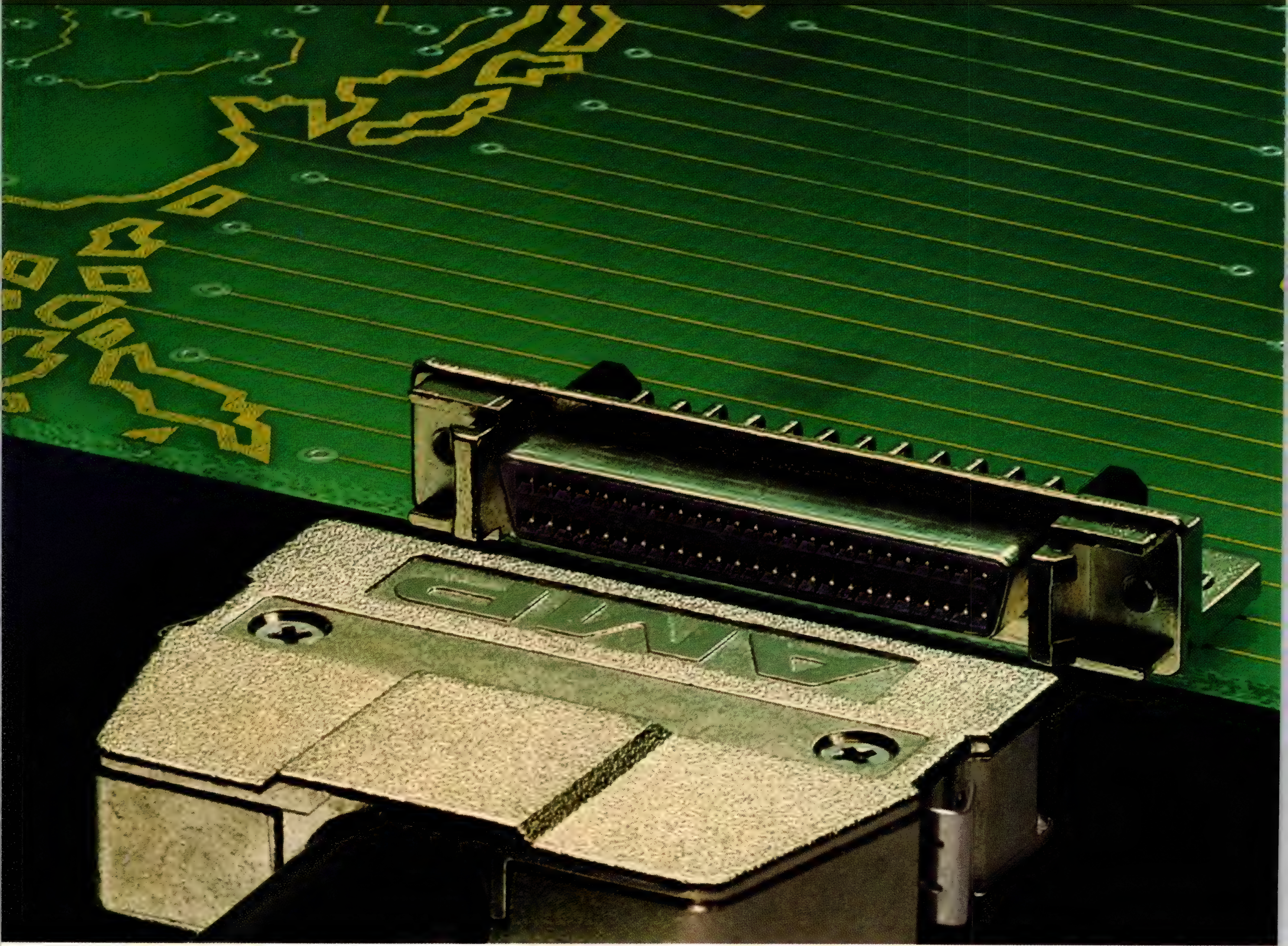

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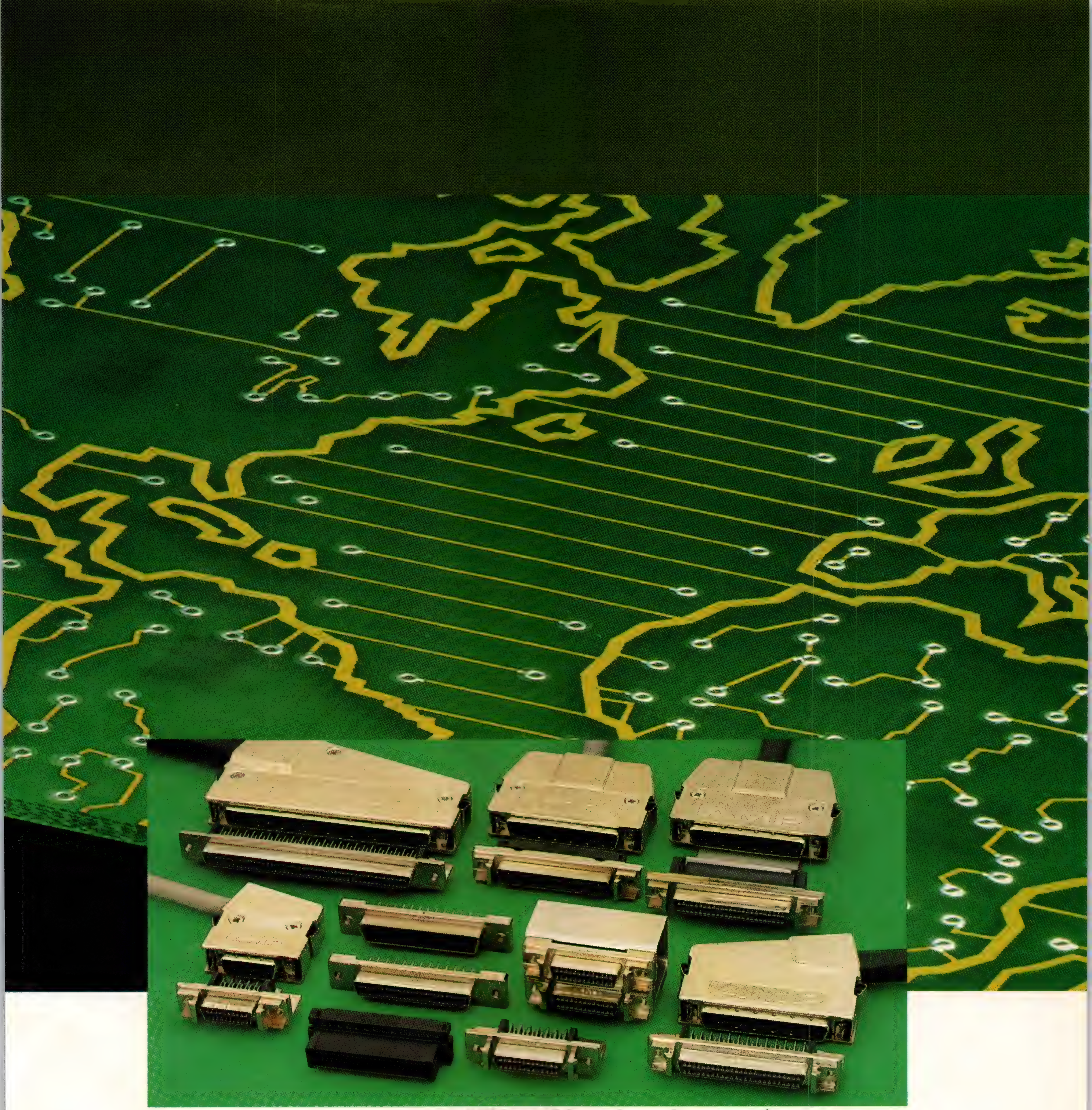

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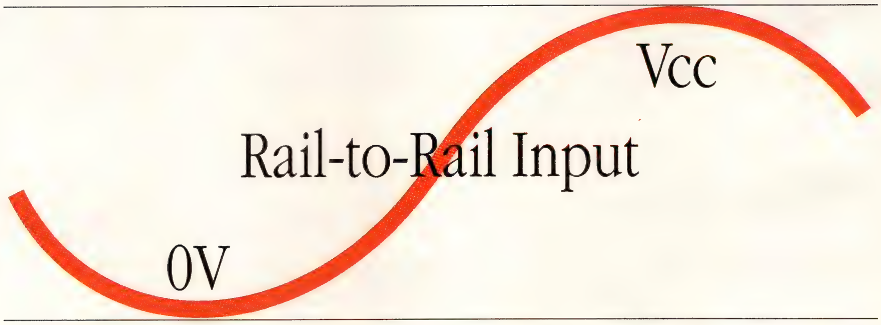

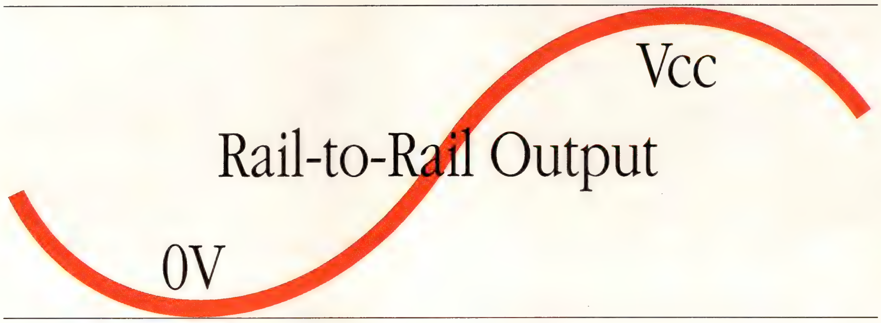

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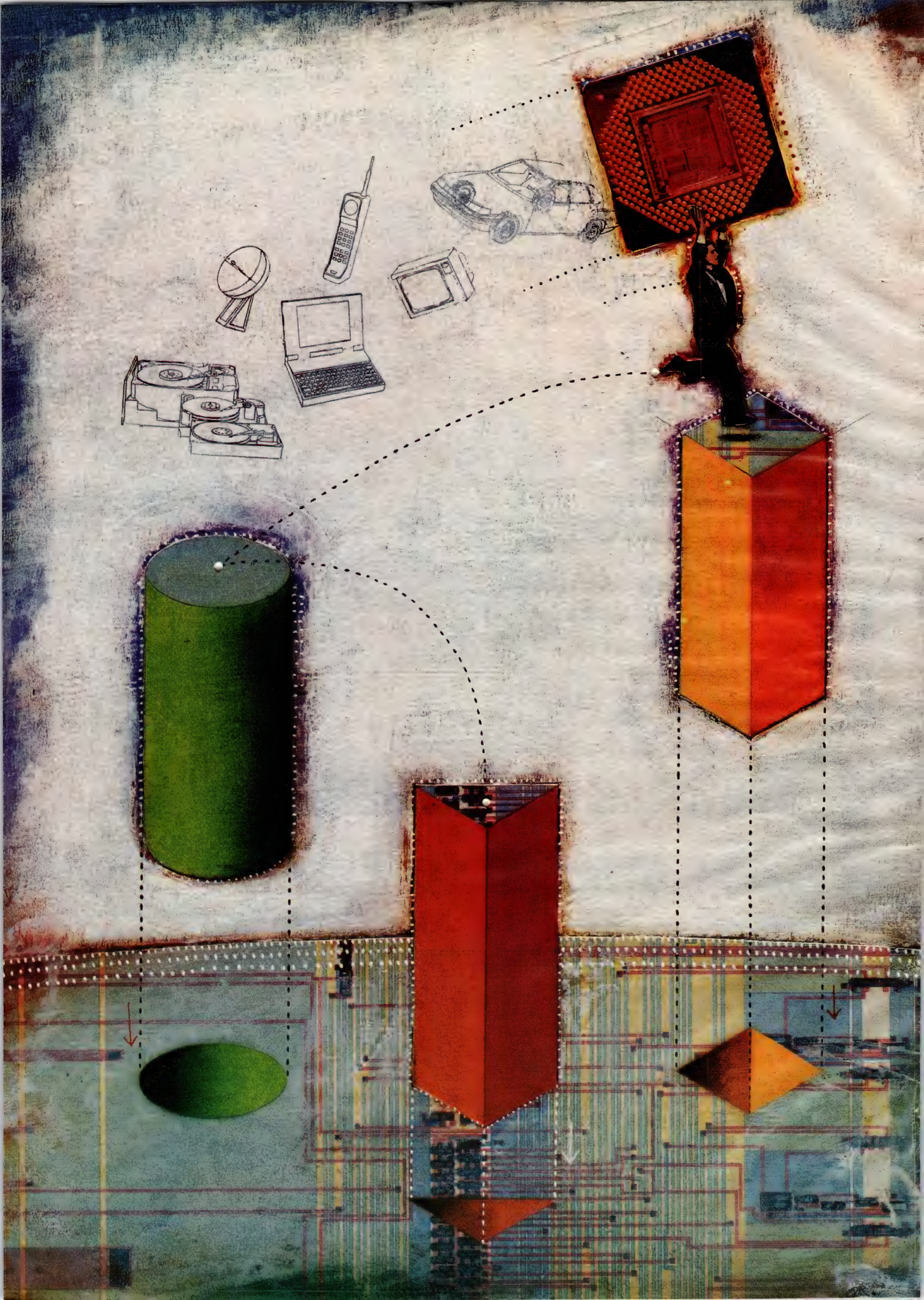

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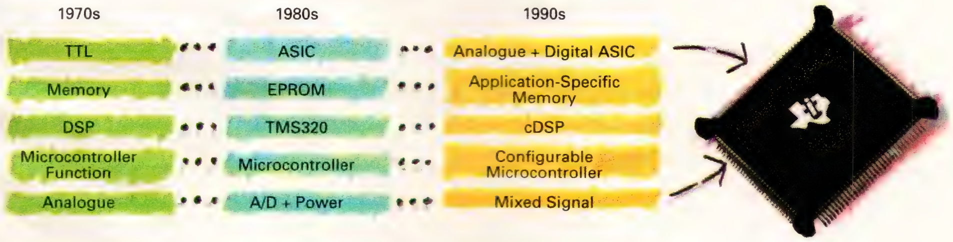

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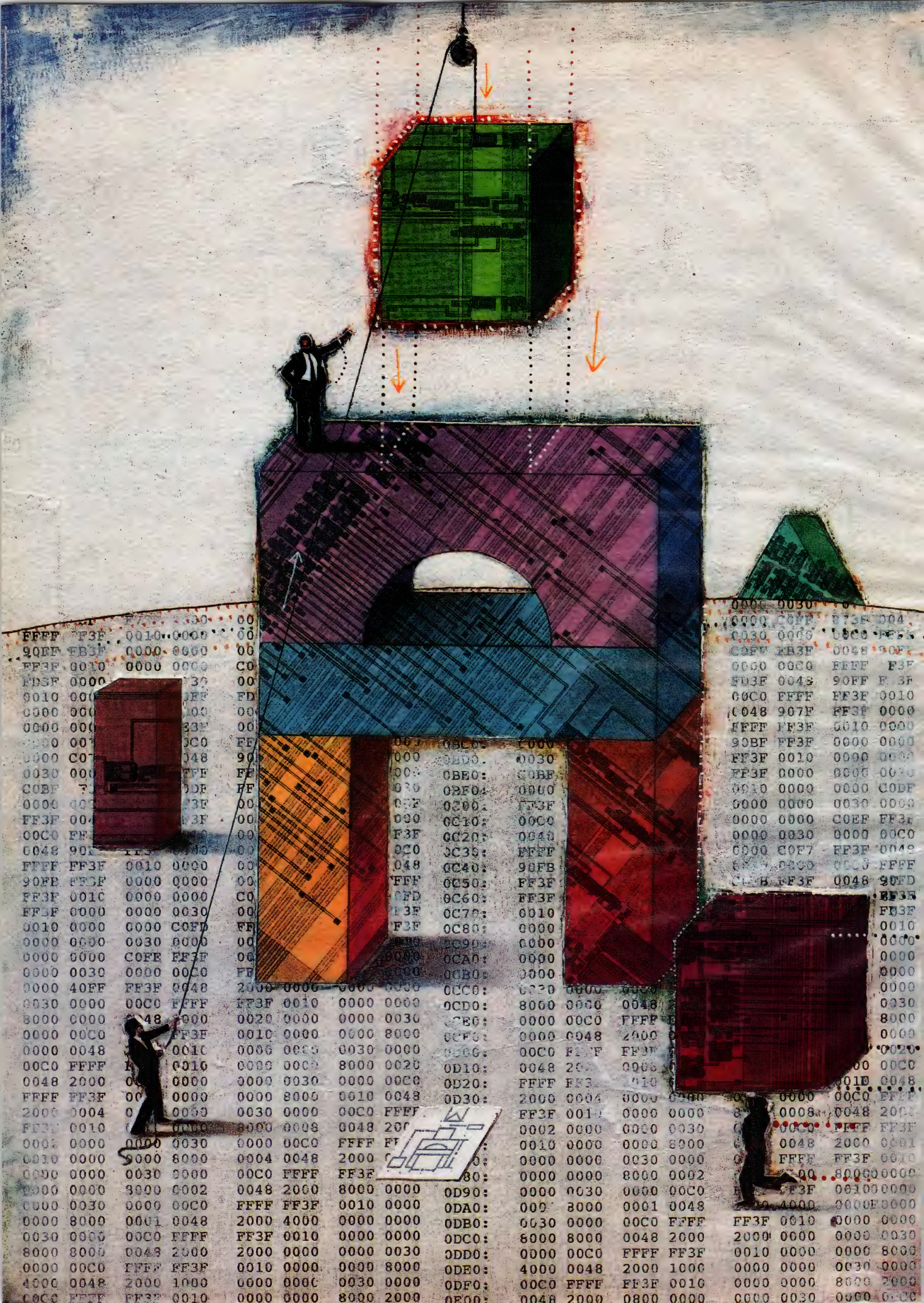

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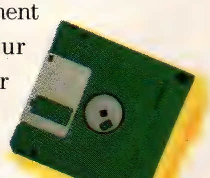

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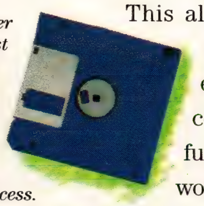

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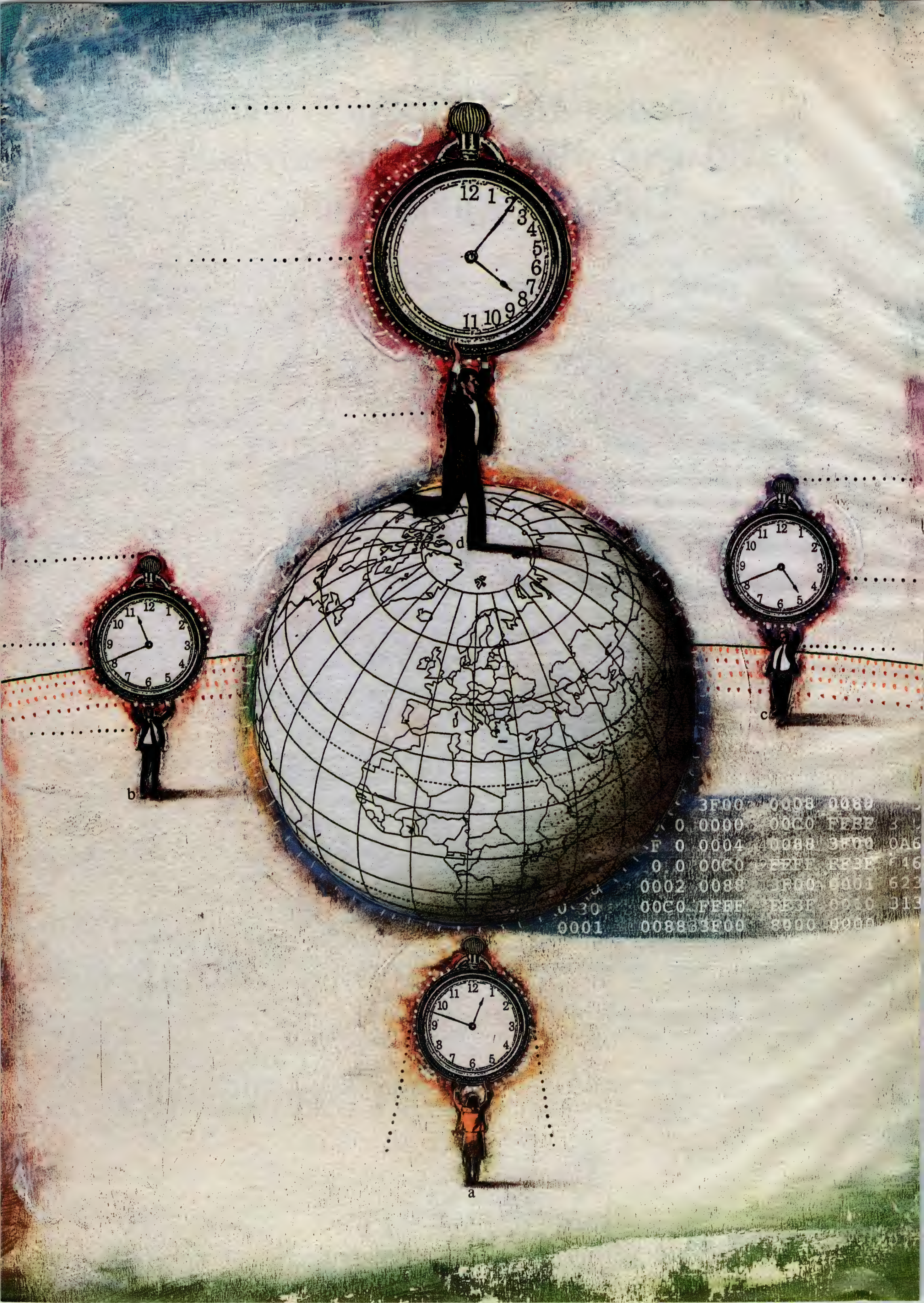
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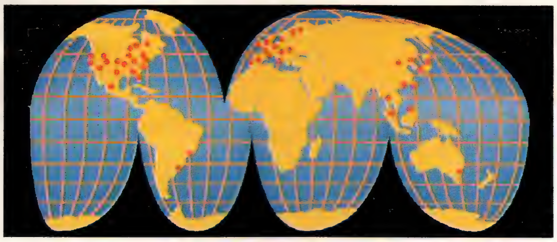

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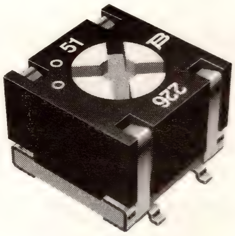

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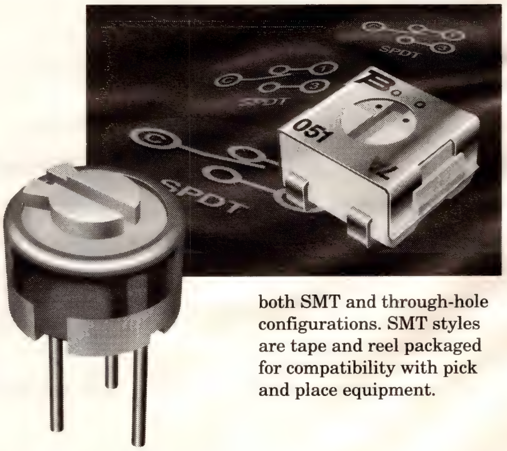

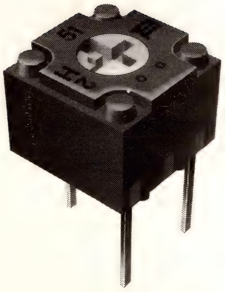

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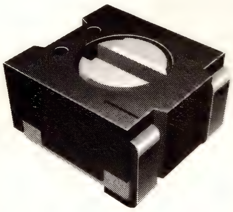

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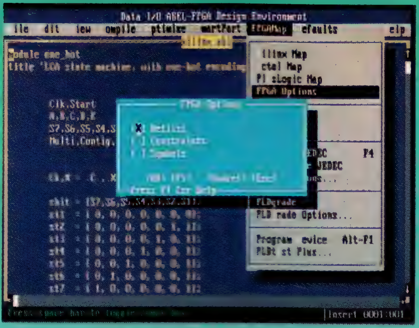

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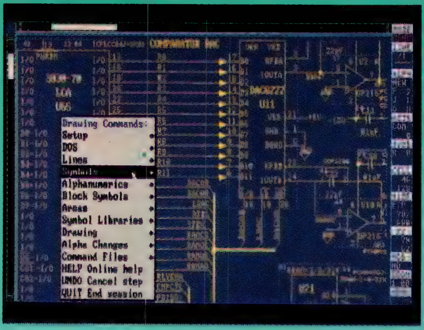

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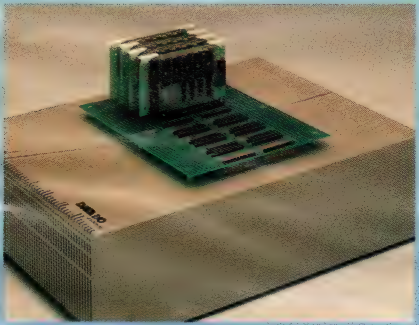

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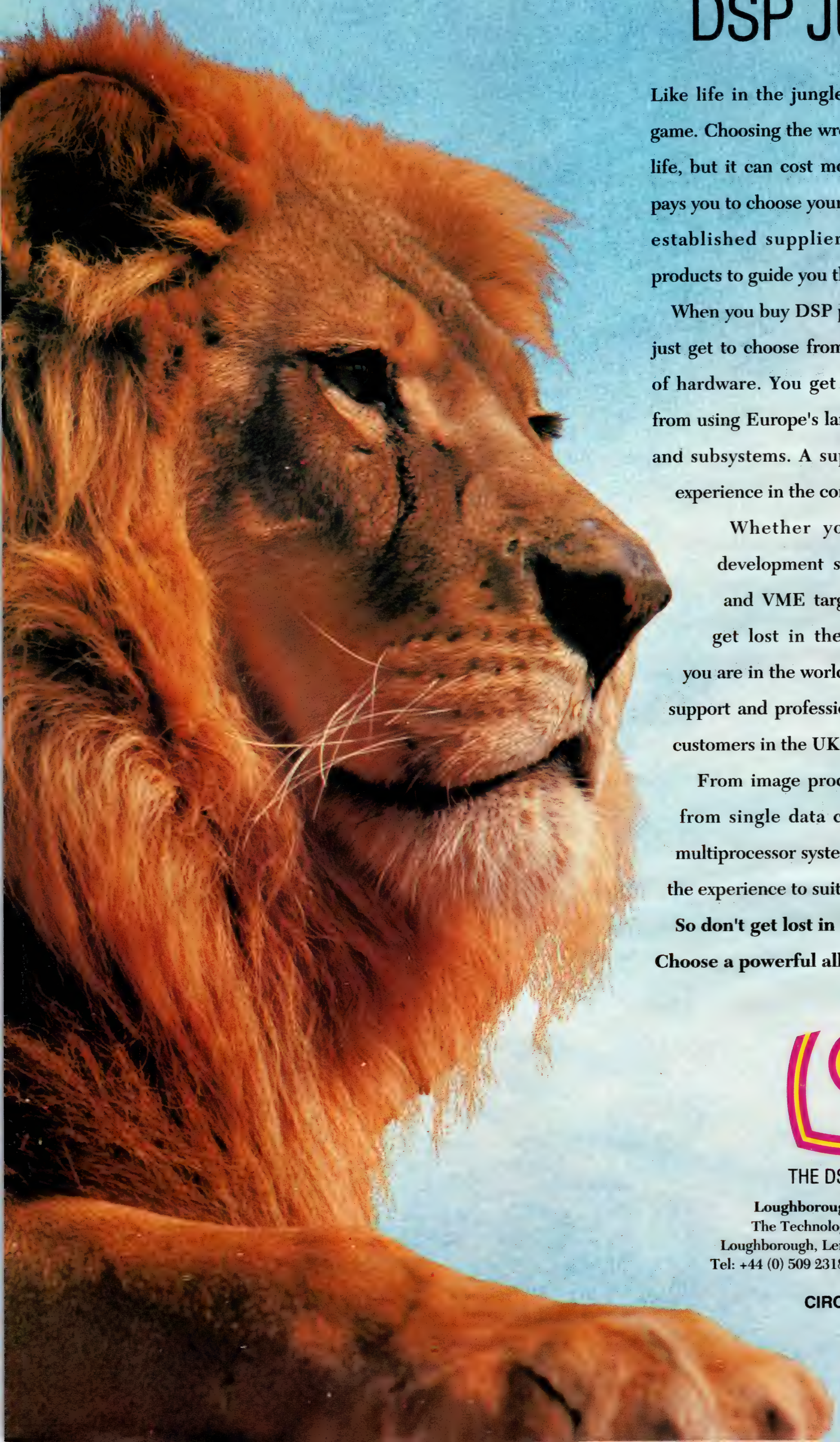

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CIRCLE NO. 160

Careful programming lets C replace assembler in fast embedded applications

JOHN DONOVAN, Managing Editor, EDN Asia

You can break the assembler habit and still write fast, small embedded applications if you follow a few simple rules.

As design cycles get shorter, it is hard to convince marketing types of the difference between writing code fast and writing fast code. Despite the pitfalls of writing embedded applications in a high-level language, the need to develop complex applications quickly leaves you little choice. By carefully optimizing your code (and resorting to a few tricks), you can write C programs that are almost as tight and fast as those written in assembler—in a lot less time.

Writing fast code is like writing slow code—it just takes more thought. To optimize your existing code, first analyze your approach to problem solving from the top down. Analyze your data and look for the fastest way to handle it to get the desired result. Only after careful analysis should you see how you can further speed up your algorithms. A fast algorithm running as part of a slow programming approach still yields a slow program; if you use compiler optimizations and tuning tricks, you'll end up writing finely tuned slow code. As Stanford's algorithm guru Donald Knuth warns, premature optimization is the root of all evil.

Listing 1 writes a pixel on a PC screen, relying on the DOS BIOS. This routine works with different screens, adapters, and video modes. However, it is incredibly slow because the BIOS routines for writing pixels carry a lot of system overhead.

Assume that your application will run on an embedded PC and will use an VGA adaptor and monitor. Because you

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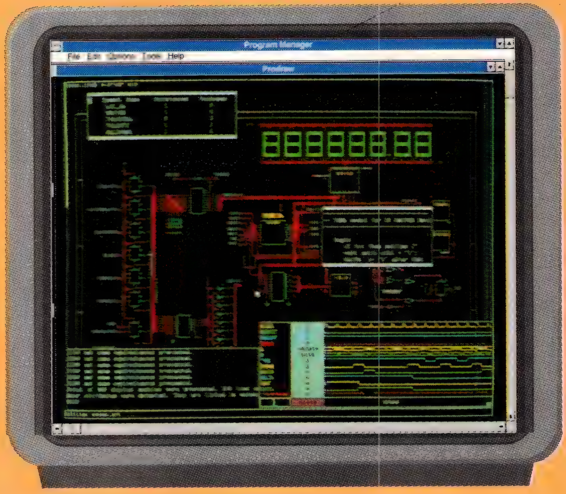

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CIRCLE NO. 47

know what hardware your application will be running on, you don't need a generalized approach. Most real-world applications write directly to the video memory instead of relying on the BIOS to draw pixels. VGA memory consists of four planes, one each for red, green, and blue, and one for intensity. Thus, each pixel requires four bits to address it (giving you $2^4 = 16$ colors)—and these bits are spread across the four VGA color planes. All four planes have a starting address of A0000H, and all are offset a fixed distance from that address. The fastest way to address a particular pixel is to use a mask that calculates these offsets and then write directly video memory, as shown in **Listing 2**.

Although more complex than the BIOS version that does the same thing, this routine executes several orders of magnitude faster. The speed results from writing directly to the video registers, whose results display immediately on screen. What you have done is trade off portability and generality for speed. What you haven't sacrificed is the low-level control you got with assembler and can still get with C.

Listing 1

```
void put_pixel(int x, int y, int color)
{
     union REGS r;
     r.h.bh = 0; r.h.ah = 12; r.h.al = color;
     r.h.dx = y;      r.h.cx = x;
     int86(16, &r, &r);
}
```

But do you really need to write one pixel at a time? More often, you need to draw lines, where the line is one color and all data points are treated the same. Instead of resetting all four registers for each point, you can initialize them once. If you are willing to sacrifice flexibility, you can gain a good deal of speed.

At the same time, think about your overall approach. The following code fills a VGA screen with color, one pixel at a time:

```
for(x=0; x<640; x++)
      for(y=0; y<480; y++)
            put_pixel(x, y, color);
```

Even the fast version of *put_pixel()* won't redeem this crude approach. Instead of filling an area with color by setting each pixel individually, you could outline the area with a line-drawing algorithm and fill it with a fast flood fill—saving a lot of time. The point is, having a blazingly fast implementation of an inherently brute-force approach just isn't good enough.

Listing 2

```
void put_pixel(int x, int y, int color)
{
 /* Place pixel at x,y in the chosen color.
    Uses mask shifting and assumes EGA/VGA color. */

 #define seq_reg_out(index,val) {outp(0x3C4,index);
      outp(0x3C5,val);}
 #define color_out(index,val) {outp(0x3CE,index);
      outp(0x3CF,val);}
 unsigned int offset;
 int dummy,mask,page;
 char far * mem_addr;
 offset = (long)y * 80L + ((long)x / 8L);
 mem_addr = (char far *) 0xA0000000L + offset;
 mask = 0x80 >> (x % 8);
 color_out(8,mask);
 seq_reg_out(2,0x0F);
 dummy = *mem_addr;
 *mem_addr = 0;
 seq_reg_out(2,color);
 *mem_addr = 0xFF;
 seq_reg_out(2,0x0F);
 color_out(3,0);
 color_out(8,0xFF);
}
```

Often, by changing your data model—or changing your algorithm to better match your data—you can dramatically speed up your application. To stick with our example, the VGA controller has different addressing modes that you can select, depending on what type of data you need to process:

- If you just want to color a pixel or a line, *put_pixel()* works fine; it uses the set/reset register to fill up to 8 pixels (one byte) of each plane with a fill color.
- If you have packed-pixel data, use the write-enable register to select the plane to modify and the mask register to determine which pixels to change; this mode works best for point and line-drawing algorithms but is notably slow for displaying stored images.

Finally, if you need to transfer data from one section of display memory to another, you can use the processor read latches to move data up to 32 bits at a time (8 bits for each plane that is write enabled) by doing successive read-and-write cycles—assuming your microcontroller (μC) can handle 32 bits at a time.

The approach you take to writing your data to the video monitor will depend on the data. You must match the tool to the task, or your results won't be satisfactory. In this case, either write specialized routines to handle your expected data or change the format you are storing your data in to handle it faster.

Finally, don't overlook optimizing your data. Tightening up your data will help save space as much as slimming down your code. Consider compressing the data; in the case of our VGA images, run-length encoding or one of several other approaches could cut the size of graphics bit maps by 75% or more. Decide if you can do without large static arrays and calculate values on the fly instead. If you have the processing speed, you may save a lot of memory. Once again, you're trading size for speed.

Once you've optimized your problem-solving approach, examine your algorithms. First use a profiler to find out where improvement is most needed. Optimize first where it matters most.

After finding out which modules take the longest to execute, look to eliminate redundant or unnecessary operations from your algorithms. When you write a function, your first aim is to get it to operate correctly. Having done that, go back and replace brute-force algorithms with faster ones. As an example of a reasonable-looking brute-force approach, the following nested loop calculates the value of x.

```
int a,b,c,d,x,y;

for(a=1; b <= 100; b++){
        for(c=1; d <= 100; d++){
                x=d*(2^b)/(y-2);
                printf("x=%i\n",x);
        }
}
```

To speed up this loop, your first reflex might be to make all the variables register *ints* and tell the compiler to optimize for speed; this yields an 8% speed improvement using the Microsoft C 7.0 compiler. However, look at the work that takes place in each loop. The value of (2^b) depends on the outer FOR loop, but does not change inside the inner FOR loop. The value of *y2* does not change inside either loop. Therefore, you could rearrange the code as follows:

```
t1=y-2
for(a=1; b <= 100; b++){
        t2=(2^b)/t1;
        for(c=1; d <= 100; d++){
                x=d*t2;
                printf("x=%i\n",x);
        }
}
```

Pulling *t1* outside the loops eliminates 9999 unnecessary calculations. Pulling *t2* outside the inner loop eliminates 99 unnecessary calculations per iteration of the outer loop. The speed-up is far more dramatic than compiler optimizations for speed and loop efficiency—40% over the earlier version in our tests. Smart programmers still count for more than smart programs.

Don't blow your stack

Every variable you declare and every function you call takes up room—often much more than you would think. Most variables have a limited lifespan, usually just the length of the function call where they are used. C sets up what it calls automatic variables on the stack. Each time a program calls a function, C creates a new stack frame or activation record for that function. The frame contains room for the function's automatic variables. The sum of these stack frames is the runtime stack, and it grows downward from high memory as the number of variables and function calls grow.

C normally passes variables by value rather than by reference; that is, it passes a copy of parameters, not letting the called routine change the original values. When one function calls another, for example

```
int function1(int one)
{
        int a=2;
        int b=3;
        function2(a,b);
}
function2(int two, int three)
```

the compiler sets up a stack frame for *function2()* that contains enough room for any automatic variables the function contains. When *function1()* calls *function2()*, the compiler places copies of *function1()*'s variables *a* and *b* in *function2()*'s stack frame. *Function2()* operates on these copies. This arrangement keeps *function2()* from possibly corrupting *function1()*'s original variables, but it also takes up more stack space—especially if *function2()* is recursive (**Fig 1**).

A function is recursive if it calls itself while running. For example, the function *factor()* computes the factorial of a number by calling itself *n – 1* times where n is the number being computed.

```
int factor(int quest)
{
int temp;
temp=quest;

if(!quest)
      temp=1;
else
      temp *= factor(temp-1);
return(temp);
}
```

Each time *factor()* calls itself, C creates new storage for the variable *temp* on the stack. If a function is highly recursive, this can take a lot of room. Try to factor a large enough number, for example, and you can easily cause the stack to expand downward to collide with the heap—the dreaded "stack overflow."

A quick fix for *factor()* is to make it nonrecursive, thus avoiding the potential for stack overflow:

```
int factor2(int quest)
{
        int temp = 1;
        int i;

        for(i = quest; i> 0; i--)
            temp *= i;
        return(temp);
}
```

You won't always be able to write your way around recursion, but do it if you can. (In addition to taking up less stack space, *factor2()* runs faster than *factor()*.) Furthermore, if you can code without recursion or re-entrance, you may be able to resort to static variables, speeding up your operations considerably.

Early 8-bit µCs handle stacks inefficiently, if at all; the burden of stack handling falls to the compiler. Byte Craft's Zilog Z80 compiler handles function calls by building a structure containing the function's arguments and placing it on the heap; it uses the heap pointer to

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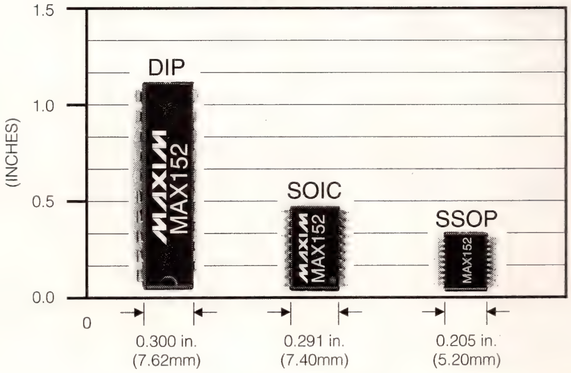

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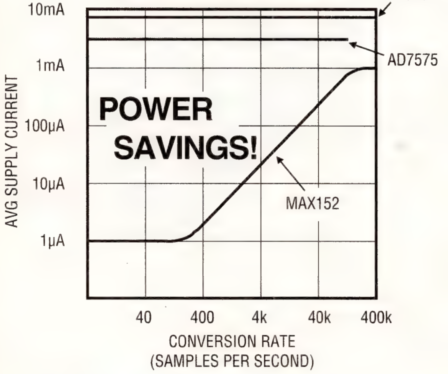

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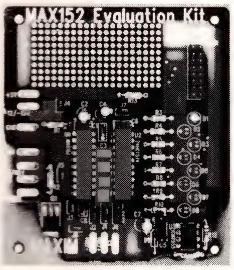

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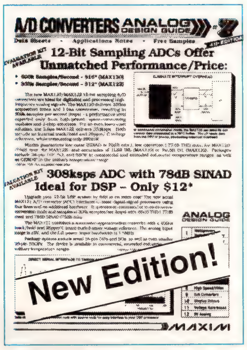

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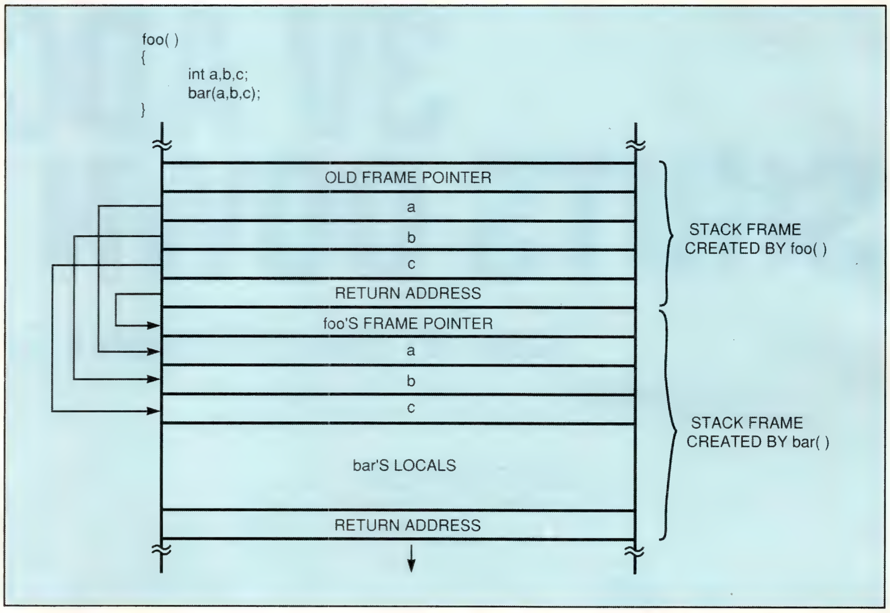
pass the arguments. This approach is the functional equivalent of what your generic C compiler does when it generates a stack. 2500AD's Z80 compiler comes with a variety of start-up programs that deal with stack handling as well as the myriad varieties of the Z80.



```
foo( )
{
        int a,b,c;
        bar(a,b,c);
}
```

Fig 1—When one function calls another, the calling function passes copies of any passed parameters (along with its return address) to the called function, which adds its own local variables to the stack. Highly recursive or nested calls can quickly overflow the stack.

Static and global variables

Factor() works properly as written, allocating stack space for each additional copy of *temp*. Because the program is working with the same variable each time, it might seem to make sense to declare *temp* to be static. Static variables retain their values between successive calls to the function. However, they don't work if a function is recursive. For example, if you declare *temp* in *factor()* to be static—creating only one copy at one place in memory—each successive call to *temp* will overwrite the previous value. With a static *temp*, the function *factor()* will always return the value 1.

Static variables are also poor choices if your code needs to be reentrant; that is, if more than one function at a time can call it (for example, an interrupt handler and a message queue) or if you intend to run it under a multitasking operating system. In the case of *factor()*, two routines could call the function at the same time as long as each set up and maintained separate stacks (the default in C). If *temp* were static, it would retain the value left over from the first calling routine when the second one called it—obviously an unacceptable situation.

In its Intel 8051 C Compiler, Programming Languages Corp (PLC) tries to speed up stack handling by precompiling stacks. Using "static frames" or "compiled stacks," PLC places all local variables and arguments in static memory. If you can live with the limitations just mentioned, this approach can speed performance considerably. Franklin Software also uses static functions exclusively in its C51 Compiler; if you insist that a function be recursive or reentrant, the compiler simulates a stack in RAM to allow for this.

All variables that you declare before the beginning of your *main()* routine are global; they exist for the duration of your program and are available to all program modules. A calling function needn't pass its values to another function; the called function can look at the global value and use or change it as necessary. The changed value will then be available to the calling function when control returns to it.

Global variables reside in high memory and remain there for the duration of the program. You could theoretically avoid passing any parameters if you stuck with globals. You can't use this trick with abandon because the number of variables in a nontrivial program can quickly eat up a huge amount of RAM or ROM. Still, don't overlook the value of globals for essential and often-referenced variables.

For its C8605 Code Development System, Byte Craft converts all local variables into globals. The development system stores the variables in global memory, letting you reuse them in different functions while still maintaining a local scope for each variable. This neat compiler trick works only with functions that don't call each other and with nonrecursive and nonreentrant functions.

If you have extra RAM, your space problems disappear. If your application has access to off-chip RAM, you can explicitly allocate memory there for stack usage or global variables (though you should store initialized globals in ROM). If you are limited to the chip's internal RAM, you may have no choice but to minimize the use of local variables, parameter passing, and function calls. Your programming choices are initially driven by problem-solving considerations, but they are ultimately limited by your choice of μC implementation.

Where you store your data can also significantly effect speed. The Motorola 68HC05, like many 8-bit μCs, devotes a high percentage of its opcode to operations in the first 256 bytes (page 0) of memory; anything beyond page 0 requires extra

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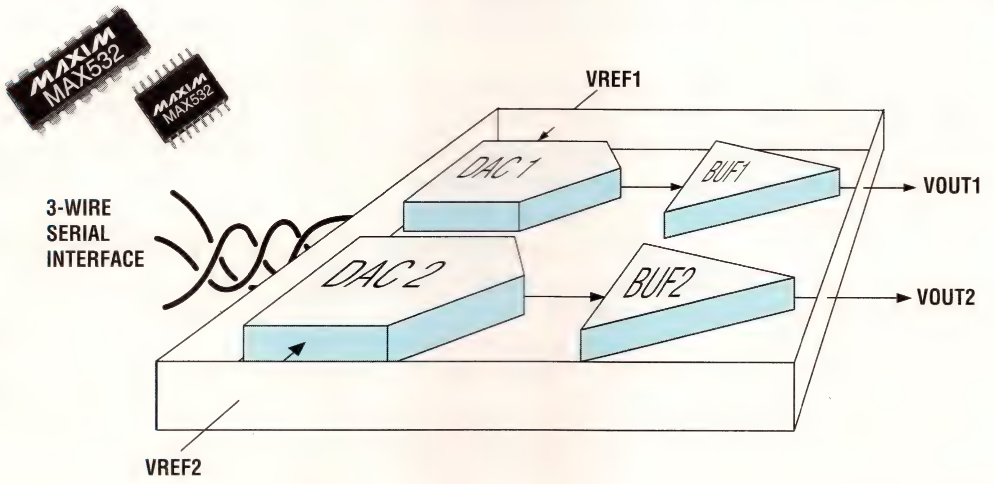

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processing. If you direct the compiler to store data in page 0 memory, your application may speed up considerably. If you cure your data-storage problems by resorting to off-chip RAM, you'll pay with the loss of speed you incur when accessing external memory.

Sometimes the speed penalty can be considerable. Archimedes Software's 8051 compiler devotes a lot of attention to code and data banking—helping you swap in code from an external memory bank. The price you pay is high, however. Bank switching on the 8051 requires 50 processor cycles and two additional bytes on the stack to implement. Obviously, you should use code banking only when you have no other choice.

Along the same lines, keep conditional branches short. Any jump beyond a single byte (whether for data or code), forces 8-bit μCs to do time-consuming calculations. A far jump, for example, requires 5 bytes of code to tell the 6805 what to do, compared with 2 bytes for a near jump. This isn't a huge difference, but it can add up.

Pointers vs indexing

Once you recognize the need to minimize stack usage, one seemingly obvious solution is to pass pointers instead of values. A pointer to a variable gives the called function the address of the variable—along with the ability to change the original variable, not just a copy. When addressing large arrays you should always use pointers because passing a copy of the whole array during a function call is too unwieldy.

However, pointers require more processing than function calls—especially if you are using an 8-bit μC and want to access a value that requires a 16-bit pointer. When working with an 8-bit μC, it may take less code to index into a fixed array than to use a pointer. The 8-bit 6805 can use an 8-bit variable to access memory without much difficulty. **Listing 3** shows the number of steps needed to retrieve a value using array indexing rather than a pointer.

Accessing data using a pointer requires almost three times the number of instructions required to access the same information using array indexing. The 8-bit 6805, however, cannot use a 16-bit variable to access memory without resorting to self-modifying code. If we change **Listing 3**'s *ints* to *longs*, pointer access suffers considerably:

```
long i, j;
int b[20];
long *ptr;
```

Now, getting the data by indexing requires 4 instructions, but retrieving the same data by a pointer requires 26 instructions—6.5 times more than needed to index into the array. The design of the 6805 limits function arguments to two bytes. The μC passes single-byte arguments in the accumulator. Two-byte arguments, such as long variables, are passed with the most sig-

Listing 3

```
0050 0051            int i, j;
0052 0014            char b[20];
0066                 int *ptr;
                     void pointdemo (void)
                     {
0100 BE 51    LDX    $51     i = b[j];  // Get data by indexing
0102 E6 52    LDA    $52,X              // into the array

0104 B7 50    STA    $50                // Requires 3 instructions
0106 A6 14    LDA    #$14    j = 20;    // Set j to 20 for
0108 B7 51    STA    $51                //   array indexing
010A A6 52    LDA    #$52    ptr = &b;  // Set the pointer to the
010C B7 66    STA    $66                     // start of the array
010E BB 51    ADD    $51     i = *(ptr + j); // and retrieve the same
0110 97       TAX                            // data by a pointer
0111 F6       LDA    ,X           // Requires 8 instructions in all
0112 B7 50    STA    $50
```

Kicking the assembler habit

To get tighter code with your high-level language, remember the following rules and apply them more or less in order.

- Rethink your approach to problems to see if you can't find a more elegant solution.
- Make sure you are storing and manipulating your data efficiently.
- Make your code less abstract and take advantage of hardware-specific shortcuts wherever possible, always weighing the tradeoffs between speed, portability, and development time.
- Optimize your algorithms, eliminating all redundant and unnecessary operations. Use a profiler and optimize where it will do the most good.
- To reduce stack usage, minimize local-variable usage, parameter passing, and nested subroutine calls. Move the runtime stack to external RAM if necessary to maximize limited on-chip RAM.
- Use in-line assembler calls for time-critical code but don't fall back on writing whole modules in assembler.

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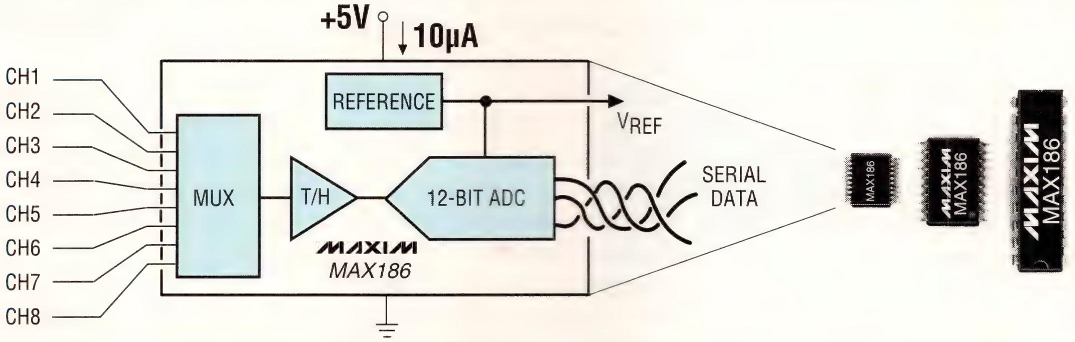

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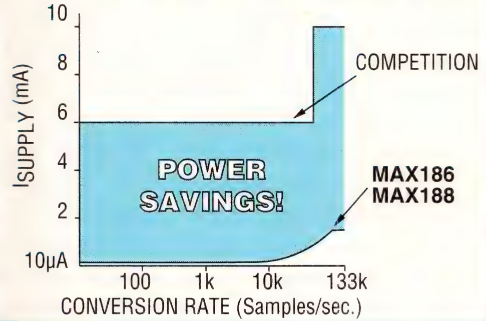

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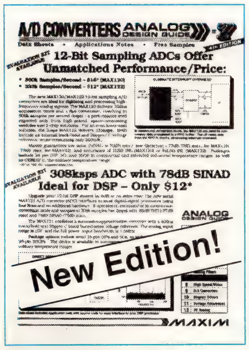
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nificant byte in the index register and the least significant byte in the accumulator. If you pass two single-byte arguments at once, the 6805 passes the first in the index register and the second in the accumulator. Further arguments are "passed" through global variables. A 6805-specific compiler knows this and generates the appropriate code—sometimes lots of it.

If pointers are no problem for your application, Franklin's C51 compiler has an interesting twist. In addition to standard 1- and 2-byte pointers, the compiler implements "generic pointers." These pointers require three bytes, one for the data type and two for the offset. A generic pointer can access any variable anywhere in the 8051's memory space. Generic pointers can be useful if you want to reuse a standard, minimal set of pointers.

Clearly, there are no free lunches. If you are using small arrays, consider either declaring them as globals or passing copies in function calls instead of using pointers. For larger arrays, you have no alternative but to use pointers and accept the reduction in speed that results.

C has some reserved keywords that can make life easier for μC programmers, including *volatile, register,* and *_inline*. These keywords tell the compiler how to treat your functions or variables. You can also declare your own keywords to work around problems.

The *volatile* keyword tells the compiler that a variable may be modified suddenly by something other than a statement, such as an interrupt handler or the operating system. The compiler won't optimize away volatile objects, knowing that their value can change at any time. This is important, for example, if the object is a memory-mapped register that is accessible by different programs or tasks.

The *register* keyword is everyone's favorite. Storing heavily used variables in registers (especially loop variables) saves memory fetches and can dramatically speed code execution and reduce program size. The effectiveness of this trick is directly proportional to the number of registers available in your target μC. Most compilers ignore this keyword once you have asked for more registers than are available at runtime.

The *_inline* keyword tells the compiler to place copies of the code for a short function every place the function is called. For example, suppose you had a function called *cosine()* that performs the following calculations:

```
float cosine(int x)
{
        float y;
        int pi = 3.1416;
        y = cos((x/pi) * 4.2)
        return y;
}
```

Calling *cosine()* from the following loop eats up time setting up and tearing down stack frames and pushing and popping values on the stack:

```
for(x = 1; x <= 100; x++)
      y = cosine(x)
```

Your program will run a lot faster if you simply substitute a copy of *cosine()* directly into the loop:

```
for(x = 1; x <= 100; x++)
      y = cos((x/pi) * 4.2)
```

This is exactly what your compiler does when you declare *cosine()* in-line. Declaring a function in-line eliminates the function call. In-lining is a direct trade of code size for speed and makes sense

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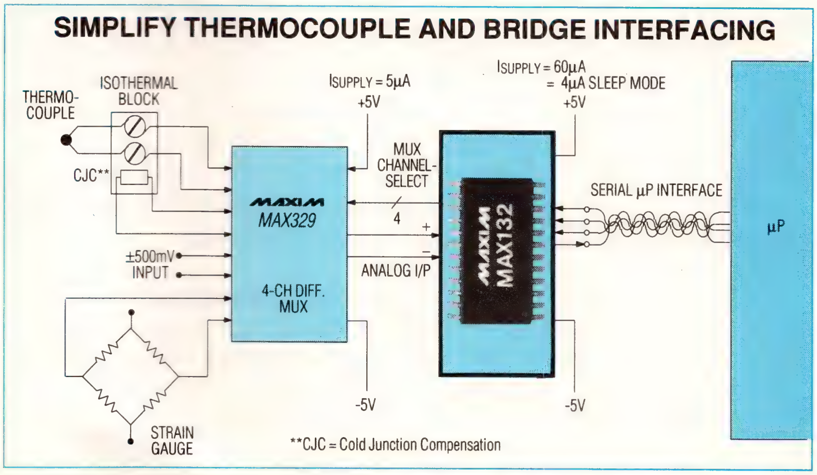

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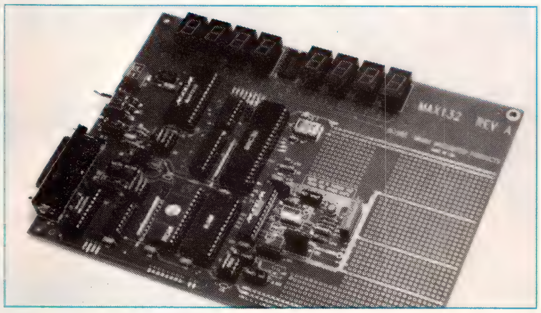

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CIRCLE NO. 65

where you have a very short function that you call often from a few points, such as the loop above. But, if you call *cosine()* from many different points, in-lining it can add a lot of code to your program.

Beyond these keywords, C keywords get compiler and vendor specific. One popular example is *_asm*. This keyword is the compiler vendor's way of making assembly programmers feel at home. The compiler converts *_asm* statements directly into assembler code. You can insert *_asm* statements inside C functions to do things that you can't normally do from C. For example, to disable interrupts while you call a function, you could write

```
foo()
{
        // disable 6805 interrupts
        _asm("sei\n");
        // call critical function
        bar();
        // re-enable interrupts
        _asm("cli\n");
}
```

All of this should reduce or eliminate the ex-assembly programmer's tendency to fall back on assembler.

Everyone wants to write the smallest, fastest code possible. The tips in this article should help you avoid writing fat, slow code. Still, optimizing one thing causes degradation of something else. Writing faster code generally means a larger program (resorting to statics, for example) and making a program smaller (using algorithmic calculations instead of reading large, static arrays) usually slows it down. Even though you can't get something for nothing, you can get code a lot tighter by paying attention to how you code. EDN

Acknowledgment

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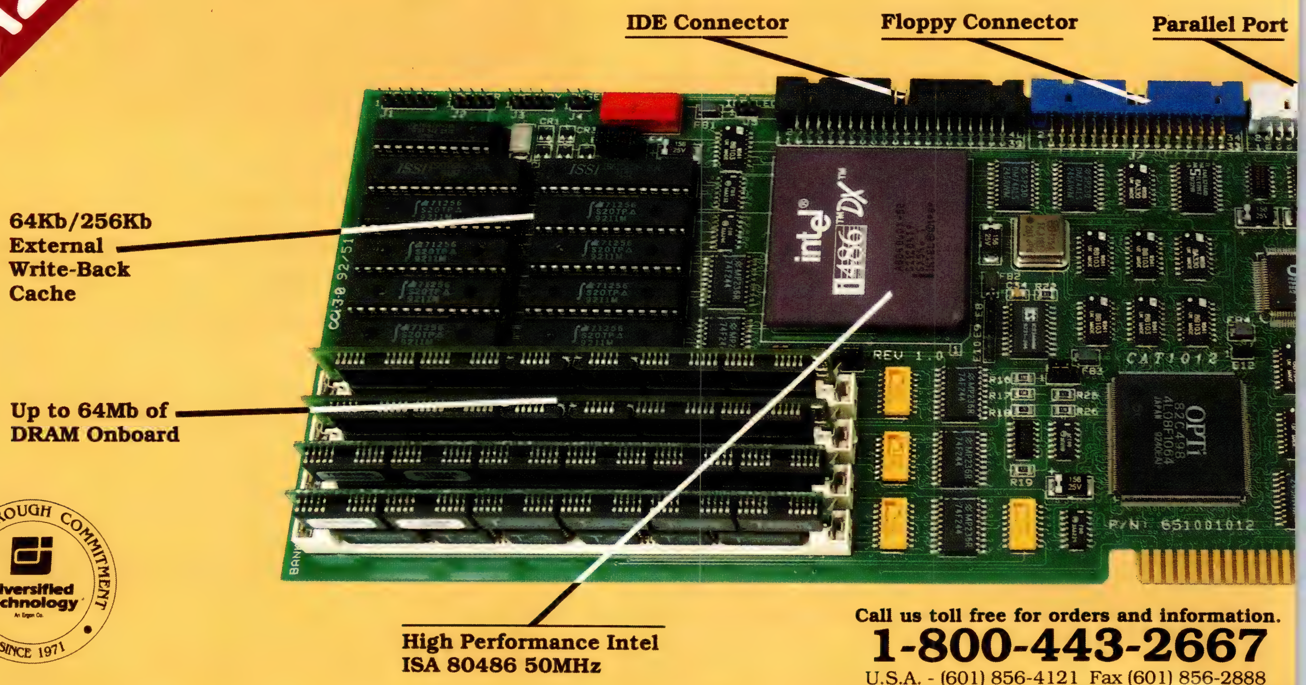
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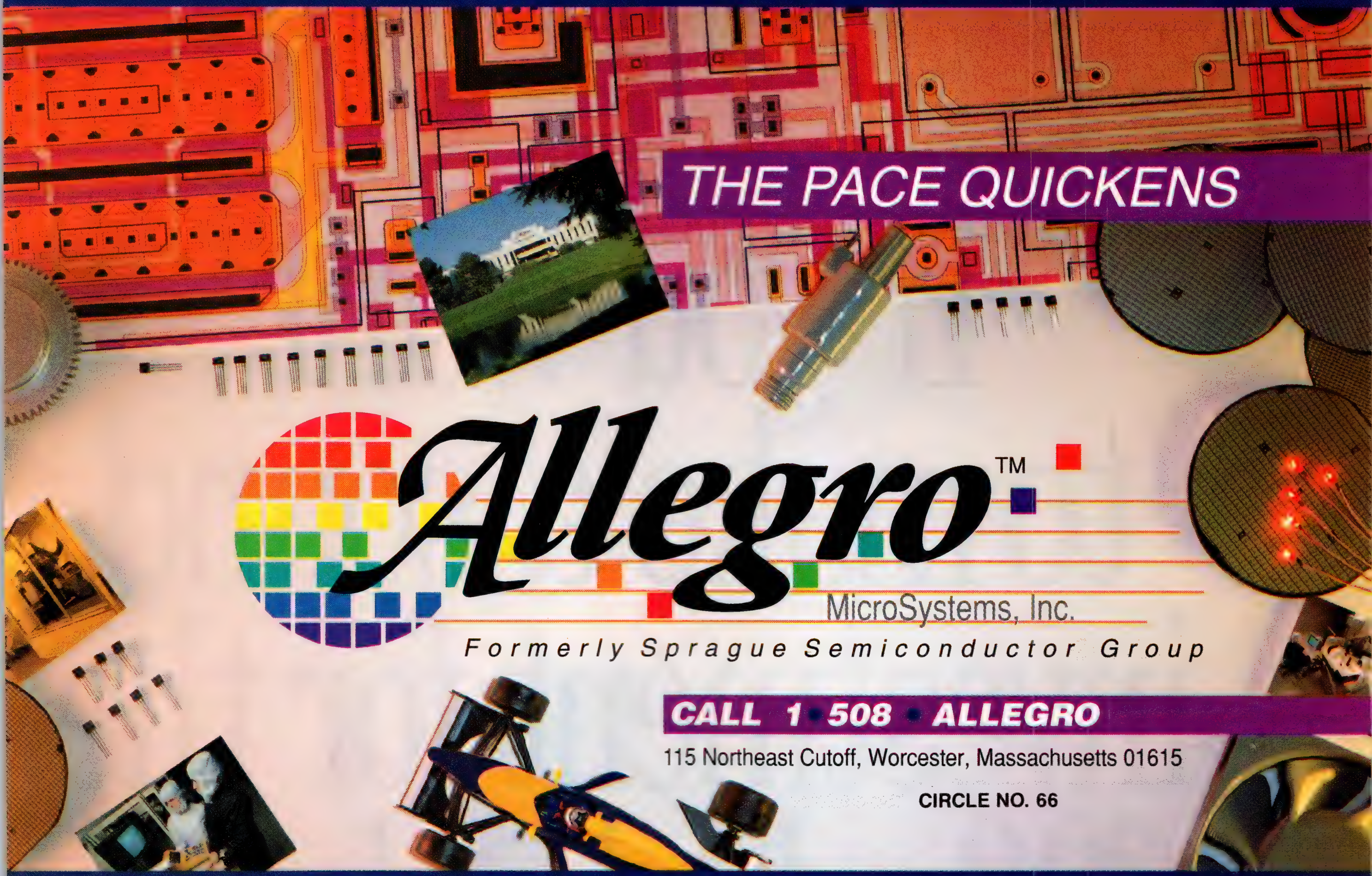

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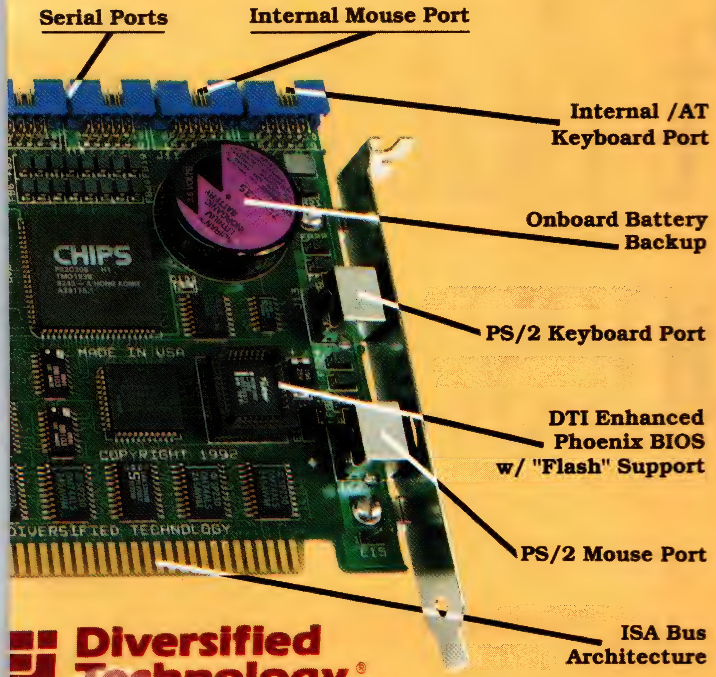

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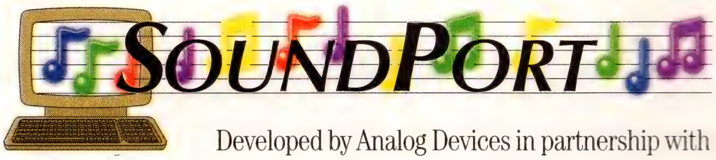

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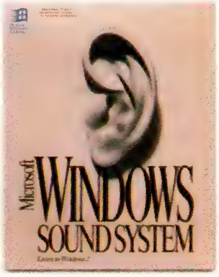

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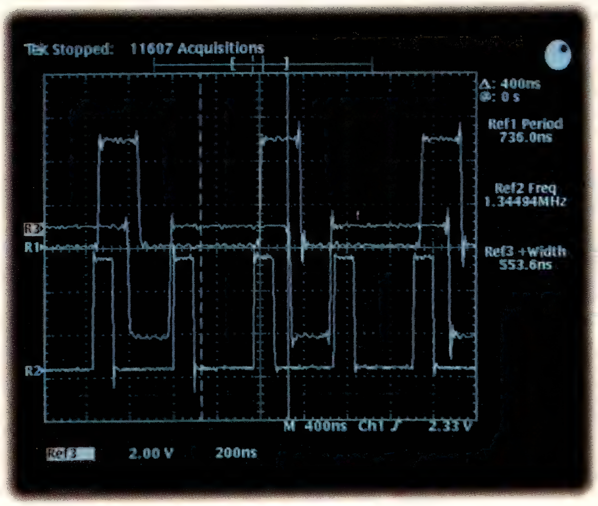

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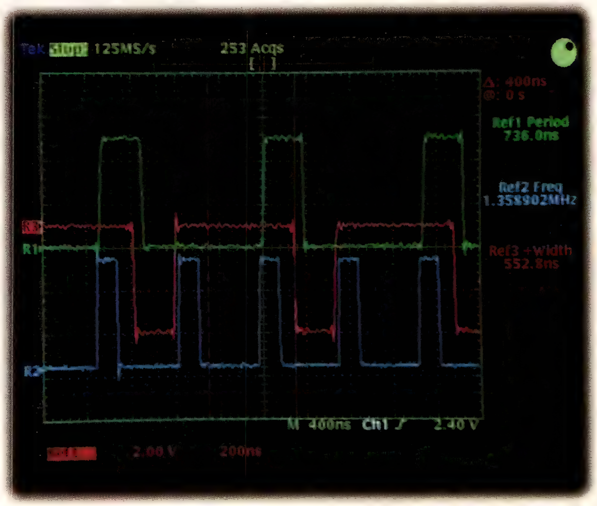

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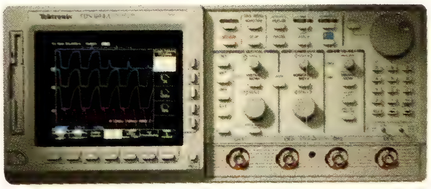

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These color scopes also come with a high-resolution monitor, a DOS compatible floppy drive so you can store personal waveforms and setups on a PC, and a VGA output that allows you to display your work on a larger monitor.

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CIRCLE NO. 35

Development tool set eases OS-9 network-software programming

A new software-development tool set, called Fastrak, from Microware Systems Corp aims to make life easier for programmers who develop software running under the OS-9 operating-system. The company anticipates that the tools will find most use in companies that use teams of software developers rather than lone programmers. Thus, the software-development tools are aimed mainly at programmers who develop OS-9-based software on a network. However, you can run the tools on your stand-alone target system, too.

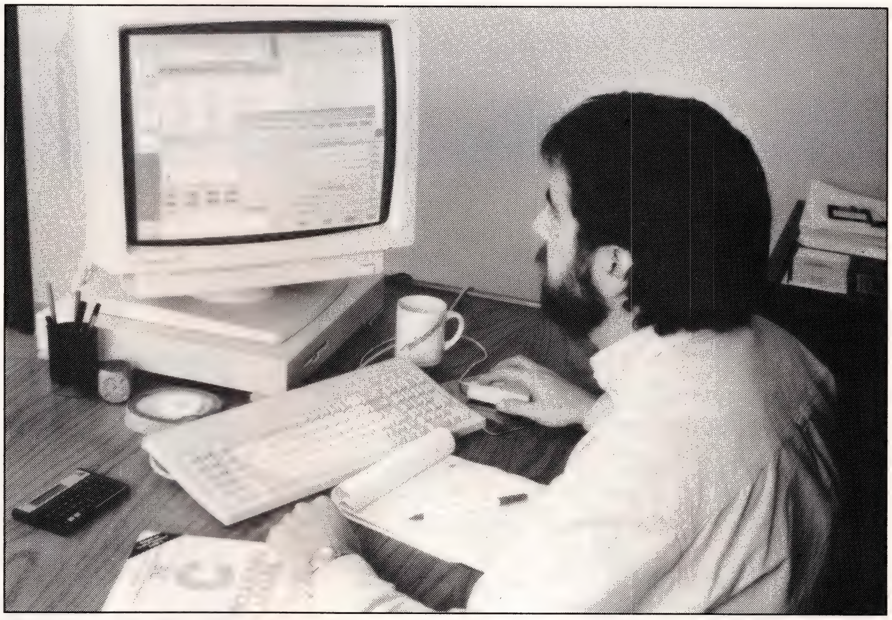
If you're using a workstation, you'll need a Unix workstation such as a Sun-3, Sun-4, SPARCStation, or HP-9000. An Ethernet/TCP-IP connection links the workstations and the OS-9 target system for which you're developing code. If you don't have a network, you can communicate between your workstation and the target system through a standard serial connection. For stand-alone operation on your target, you must have a 680x0-based computer that runs OS-9. The Fastrak software supplies an X-Window/Motif user interface.

The system includes five tools; Fastrak Workbench, Text Editor, Makefile Editor, Fastfix Debugger, and Target Monitor. The workbench lets you manipulate files and directories, set your operating preferences and defaults, and start other software tools. You can also access the version-control software and automatically build and execute programs. All file-access operations go through the version-control portion of the system to ensure the integrity of source-code files. At any time, you can save the "state" of your workbench, which lets you switch to another task and return to your software-development task just as you left it.

The editor is fairly standard, but it offers the ability to change code as errors occur during compilation and linking. For example, if the software detects an error as you're "building" an application, the software automatically displays your code within the editor, highlighting syntax errors so you can change them. The editor includes definitions for *vi* and *emacs* editors, and you can add new definitions to get it to emulate other popular text editors.

The debugger resides in the host computer, but you use it to remotely control the execution of software on your target application. The debugger lets you operate with either C source code or assembly-language instructions, and you can display both simultaneously. You can also open windows that show you the contents of CPU and floating-point-unit registers, local variables, stack frames, and target-system memory locations. If you want to recall a debugging session, you can save command files for review later.

The tool set includes the company's Ultra C complier, which features local, global, and interprocedural optimizations. In addition, the compiler complies fully with the 1989 ANSI and 1990 ISA/IEC specifications for the C language. Prices range from $3750 per system for the version that resides in your target computer to $14,500 for five networked workstations. The company plans to have a Windows/DOS version of the software available in mid 1993.—**Jon Titus**



The Fastrak software lets you develop software on your workstation for OS-9-based computers. Integrated tools provide for editing, building, and debugging application software.

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Touch-memory chips act as silicon labels that expand your LAN

The $75 DS9092K Touch Memory Starter Kit teaches you how to extend your LAN to include doorways, bins, boxes, and even people, as data sources. To do this, the kit provides an assortment of software drivers collectively named the Touch Memory Executive (TMEX). The software lets your computer access and alter the 4-kbit, nonvolatile data capacity of the included touch memory buttons as easily as it can access a disk drive.

Each touch-memory device contains a network controller that you can manage with the software via your computer's COM port. You can use a single-wire bus for serial connections among hundreds or even thousands of these devices, each of which contains a unique registration number. This unique identification lets the software establish a private communication channel with one or more devices at data-transfer speeds reaching 16,000 bps. A search algorithm embedded in the buttons facilitates polling.

The software includes application programs and libraries that run under Microsoft Windows and DOS. A tutorial program introduces you to the multifaceted nuances of touch memory and an assortment of applications. As a professional programmer's tool, the software is compatible with a variety of languages, including C++, Pascal, and Visual Basic. The software can also call functions in Windows 3.1's Dynamic Link Libraries.

The stainless-steel housing that surrounds each touch-memory button lets data flow directly through the lid of the enclosure. An adhesive backing lets you attach devices to virtually anything and change their data contents without removing them from the item they're stuck on. These chip-based electronic labels can facilitate digital data flow between islands of automation previously inaccessible by a computer network. This tracking ability lets you track work in progress and even the location of employees.

The simplicity of the software's data-reader is perhaps one of the system's most attractive features. Instead of the complex optical scanner required for reading bar codes, you can read a touch memory with an inexpensive metal conductor. You can read or write a memory device that is 100m away from your terminal by extending the length of the conductive surfaces leading to it. Other advantages gained by using these silicon labels instead of traditional ink-on-paper include the large amount of data each chip can hold, the random access of that data, and the durability of the steel case.

The kit includes five touch memories, a probe, a tactile feedback device, an RS-232C port adapter, different types of mounting hardware, a brochure entitled "5 Steps to Touch a Memory," a demonstration diskette, a booklet entitled "50 Ways to Touch Memory," and a set of TMEX disks and documentation. The software runs on MS-DOS computers; Windows 3.1 is not necessary for operation.—**JD Mosley**

This touch-memory starter kit lets you string several nonvolatile devices along a single wire and independantly access or change the information stored within via your computer's LAN or COM port.

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Dual-block PLD architecture offers speed and density

If your design uses multiple 22V10s or other low-density PAL devices that you'd like to integrate into one high-density PLD, typically you have to overcome a couple of obstacles. First, you need a high-density PLD that can meet the design's speed and density requirements, and second, you need an easy way to transfer your design to the new device.

Xilinx's XC7300 family of PLDs and its XEPLD translation software let you convert lower-density PLDs into one IC, which saves space and power, increases reliability, and reduces cost. The PLDs have a dual-block architecture, which accommodates applications that require a small portion of the design to run at high speeds while the remainder operates at slower speeds.

Xilinx plans to introduce all five members of the XC7300 family by year's end. All versions will have densities spanning from 4 to 16 function blocks. The XC73108 is available now. It has 12 function blocks, which is roughly equivalent to 12 22V10 devices. Two speed grades are available: A 15-nsec-max, pin-to-pin version costs $45.25 (84-lead PLCC) and a 12-nsec pin-to-pin version costs $67.75 (1000).

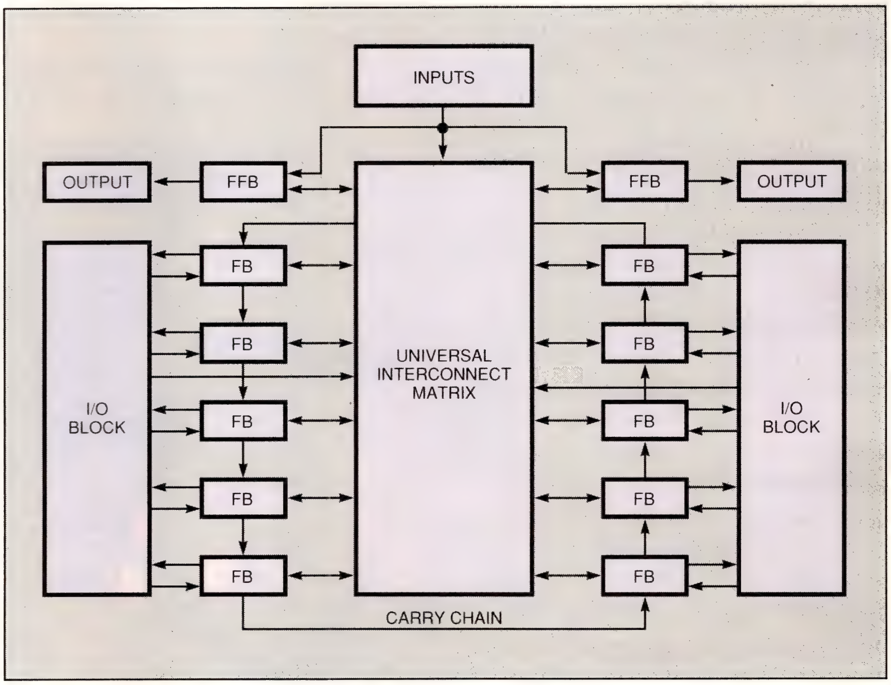
Two fast-function blocks (FFBs) on the XC73108 offer 12-nsec pin-to-pin delays for operation to 80 MHz. The FFBs have 24 inputs, an AND array that generates 45 product terms, nine registers, and nine outputs. You can program the FFBs to perform functions such as an 80-MHz, 8-bit loadable counter, an 80-MHz state machine, or a 12-nsec, 12-bit memory decoder.

The rest of the XC73108 uses high-density function blocks, each with 24 inputs, 57 product terms, nine registers, and nine outputs. The function blocks have a dedicated ALU that speeds adders and comparators. The ALU has a 9-bit lookahead-carry feature to improve speed on wide operations. A carry chain propagates carries through all high-density function blocks. Using the function blocks, you can program *n*-bit up-and-down counters, 55-MHz synchronous state machines, or 35-MHz, 18-bit accumulators.

A universal interconnect matrix that offers 100% interconnect with a single fixed delay connects both the FFBs and the high-density function blocks on chip. The matrix guarantees that if a design maps into the PLD, it will route.

The UV-erasable XC73108 has 3.3 and 5V I/O capability and power management, which provides a low-power mode when maximum speed isn't required. Representative current levels for the XC73108 range from 150 mA in low-power mode at a low clock rate to more than 350 mA in high-performance mode.

The XEPLD translation software provides simple translation of the logic equations into the XC7300 family. You can also directly import JEDEC files for translation. To convert a design, you enter or import the multiple PAL descriptions into the design environment. You also need to designate which functions, if any, you need to map into the FFBs. The software automatically maps the logic into the chosen device, and an automatic partitioner optimizes and partitions the design. The software offers a direct interface to standard PAL compilers. The software costs $995. Schematic design entry is also available.



Two fast function blocks (FFBs) on the XC73108 operate as fast as 80 MHz; the other 10 function blocks (FBs) are limited to 55 MHz. Each function block contains nine macrocells, for a total of 108 on the EPLD.

—Doug Conner

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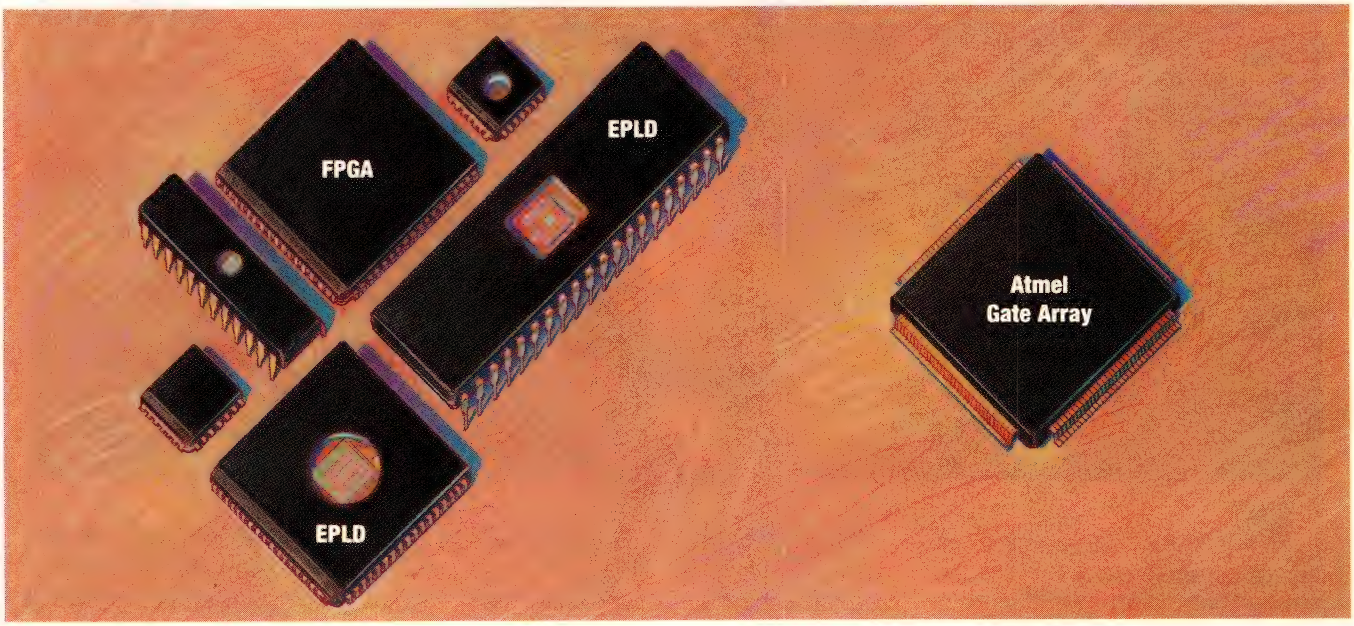

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CIRCLE NO. 72

VHDL software speeds simulation

If you're trying to simulate large designs that you've written in VHDL (VHSIC Hardware Description Language), the Leapfrog Simulator may speed your work. Cadence Design Systems Inc says that the Leapfrog simulator typically runs from 10 to 20 times faster than competitive products; the key is native compiler code.

Most VHDL simulators run by producing pseudocode (p-code) or C-language code. The pseudocode is aimed at a pseudocomputer that doesn't actually exist. The pseudocode is later interpreted or compiled into code for a specific computer. By using a pseudocomputer structure, manufacturers can get to the intermediate p-code step quickly and can then write interpreters or compilers for specific computers. However, there is a penalty: Translating the p-code to operate on a specific computer can be a bottleneck.

The C-code approach translates the VHDL code into C-language statements that you must compile and link on your workstation. It's up to you to provide the C-language tools. Sometimes, VHDL-simulation code can be too large for the compilers to accommodate, so you must break your code into pieces—a needless and time-wasting headache if you're trying to get quick simulations.

Cadence takes an alternative approach by generating native code that runs on your computer without any intermediate code-generating steps. The company claims that because its software can generate machine code tailored for VHDL event-driven simulations, you get faster simulations. The Cadence approach also eliminates size restrictions on the compiled VHDL code. The company supplies a set of benchmarks that compares the Leapfrog simulator with other simulators.

A floating license for the Leapfrog software costs $43,750, but if you already use the company's VHDL-XL simulator, the upgrade is free. The VHDL simulator complies fully with IEEE-1076. To run the software, you'll need a Sun SPARC-based computer. The company expects to offer versions for HP and IBM workstations later in 1993.—**Jon Titus**

Cadence Design Systems Inc, 555 River Oaks Pkwy, San Jose, CA 95134. Phone (408) 944-7400. FAX (408) 435-9585. **Circle No. 387**

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CIRCLE NO. 73

Wirewrap breadboard uses adjustable analog and digital modules

This may be the age of desktop engineering, but benchtop design is not dead. Designers still need to get real circuit feedback by breadboarding their designs. The Smartpro system from Circuit Tree moves breadboarding from wirewrapped components to modular prototyping. With Smartpro, designers build circuits using adjustable analog and digital modules, which plug into a wirewrap mother board.

Most engineers breadboard prototype circuits using wirewrap boards, which connect a circuit's basic components. This method has problems: Complex designs are difficult to breadboard this way, and single-level wiring can lead to hard-to-cure ground and voltage loops.

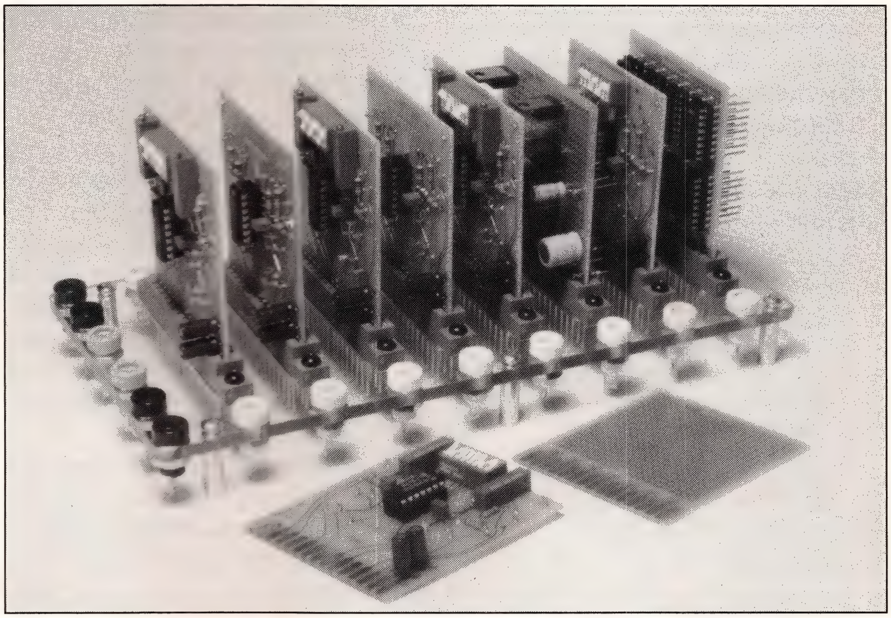
Smartpro steps up from component-level breadboarding by combining modularity and programmability. The system consists of more than 50 analog and digital modules and a mother board. The basic 5×8-in. mother board has eight 30-pin connectors to hold the 2½×2½-in. modules. For larger designs, you can chain together two mother boards using modules with two edge connectors. Each mother board is prewired for power and ground and has separate digital and analog buses. Each module pin can carry up to 3A dc.

You build your design by selecting the modules you need and configuring each module for its specific circuit function. Unlike a standard breadboard, you only have to wirewrap the connections between the modules themselves. Each module comes with a combined data sheet and application note, which lists the theory of operation, tested parameters, and performance limitations.

Most of the system's modules are analog, but there are some digital modules for digital control and interfacing to digital outputs. Analog modules include quad op amps, precision amplifiers, comparators, filters (multiple feedback, switched capacitor, and voltage controlled), ADCs, DACs, function generators, and motor drivers. Other analog modules are multipliers, peak detectors, phase-locked loops, power supplies, pulse-width modulators, rms-to-dc converters, S/H circuits, stereo amplifiers, multiplexers, 555 and 7555 one-shot timers, voltage references, and voltage-to-frequency and frequency-to-voltage converters.

A typical analog module has one or two adjustable potentiometers and an 8-pin DIP switch to configure module functions. For example, you can configure an op-amp module as an inverting or noninverting amplifier, a voltage follower, difference amplifier, integrator, single-supply amplifier, or summing amplifier.

Digital modules include crystal oscillators, counters, comparators, decoders, debouncers, phase-locked loops, digital word generators, flip-flops, gates, line drivers and receivers, multiplexers, and registers. Blank modules are also available for you to create your own daughter boards. These boards have 476 double-plated through-holes for mounting discrete components and can accommodate eight 16-pin IC sockets. A modified blank module has an additional 42 soldering posts for discrete components.



You can breadboard your analog/digital design using adjustable modules that plug into a wirewrap mother board. The modules keep the wiring clean, thus minimizing ground loops and noise.

The mother board costs $79. A blank module costs $8; function modules are $30 to $60 depending on the card's complexity. The board, blank modules, and some analog and digital modules are available now. By July, 50 module types should be available.—**Ray Weiss**

Circuit Tree, 27402 Via Caudaloso, Mission Viejo, CA 92692. Phone (714) 454-2208. FAX (714) 454-1607. **Circle No. 389**

Real-time OS keeps up with POSIX standard

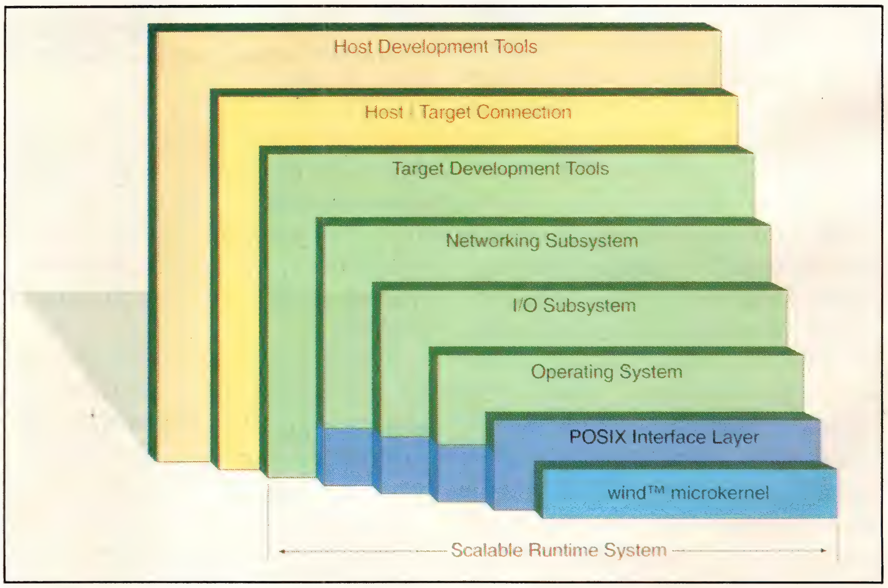
In addition to its existing POSIX.1-compliant (Portable Operating System Interface) functions, VxWorks 5.1 provides several functions from the emerging POSIX 1003.4 real-time extensions. The added features include signals, clocks, and timers. The company expects to deliver full 1003.1 compliance by early 1994.

The POSIX 1003.1 standard provides a small set of basic Unix system calls that has already achieved ISO sanction and ratification by the IEEE development committee. The 1003.1 standard, however, does not address all of the features required for real-time systems. The Real-Time Extensions subcommittee, 1003.4, is currently specifying real-time task management, communications, and I/O facilities.

Some of the features the committee is defining include priority scheduling and pre-emption, binary semaphores, clock and timer facilities, interprocess communications, real-time signal extensions, asynchronous I/O, real-time files, shared memory, and memory locking. VxWorks 5.1 implements two of these nine items. The manufacturer expects to make its product compliant with the remaining 1003.4 standards soon after ratification, toward the end of 1993.

POSIX has a set of Unix-based facilities and calls that lets products from multiple vendors work together. VxWorks is a Unix cross-development package that networks workstation-hosted tools for design, testing, and debugging with target hardware running the *wind* microkernel operating system. Target processors include Motorola 68000/68300, SPARC and SPARClite, Intel 80960, and Mips R3000. 10-user license, $22,500.—**John C Napier**

Wind River Systems Inc, 1010 Atlantic Ave, Alameda, CA 94501. Phone (510) 748-4100. FAX (510) 814-2010. **Circle No. 313**



This integrated series of cross-development tools, VxWorks 5.1, includes POSIX-compliant pipes, signals, clocks, timers, an I/O system, and directory handling.

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CIRCLE NO. 74

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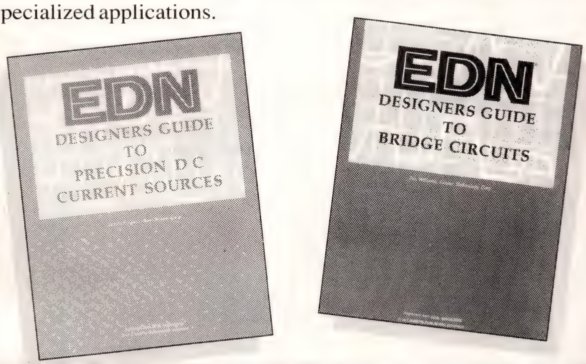
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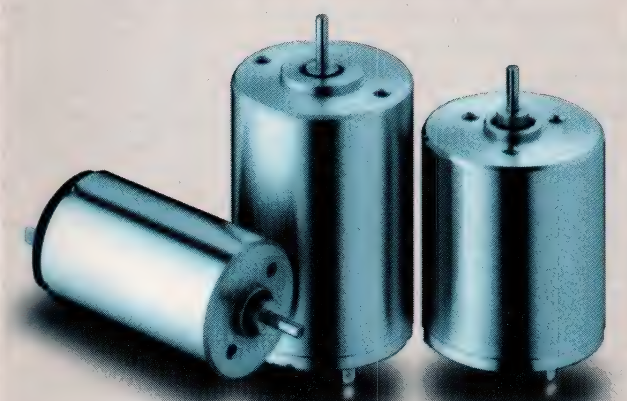

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CIRCLE NO. 76

Transputer hits 50 MHz, goes superscalar

SGS-Thomson's Transputer has gone superscalar, joining the upper ranks of high-throughput RISC processors. The new T9000 has a 5-stage, flexible pipeline and can issue up to eight instructions per clock cycle from its second-stage decoder/grouper. The 32-bit T9000 delivers a peak performance of 200 native MIPS or 25 Mflops.

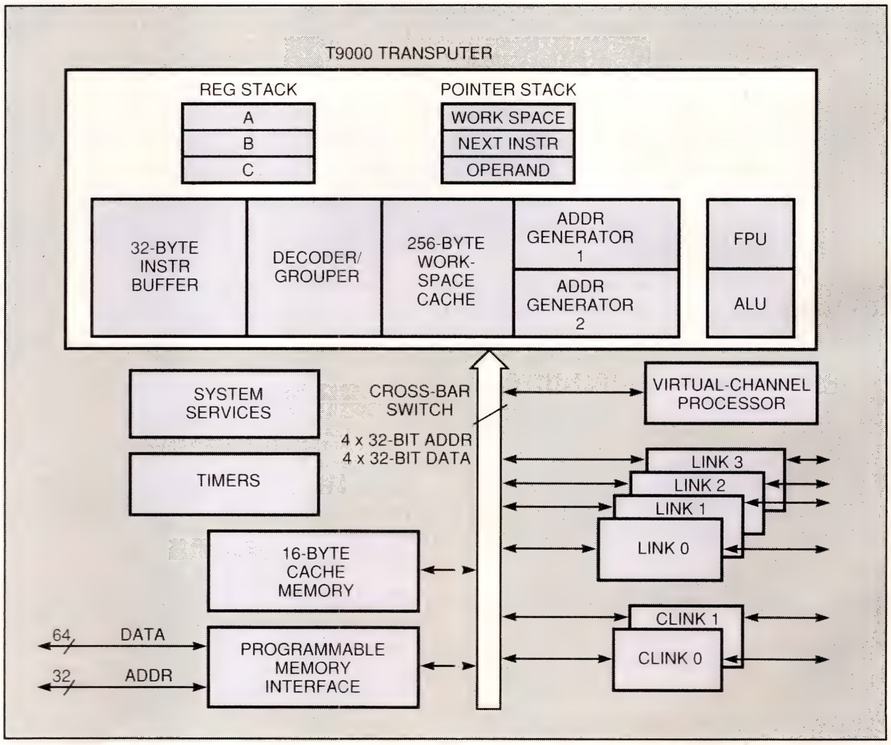
One of the first 32-bit μPs, the Transputer integrates an innovative stack-oriented architecture with hardware-based multiprocessing. The T9000 upgrades the architecture by adding RISC-like features for speed and virtual channels with small packets for high-speed serial communications between processors.

The T9000 is not a pure RISC machine, but most operations are implemented in logic rather than microcode, and the processor has a minimal instruction set, minimal number of addressing modes, and a pipelined CPU. However, unlike RISC processors, the T9000 has variable-length instructions, uses complex instruction sequences to build constants for processing, and programs special functions in microcode to increase code density.

The T9000 designers extended the original Transputer's 2-wire serial links by moving from point-to-point channels to virtual peer-to-peer channels that use wormhole routing. They also provided full-duplex operation with four wires per link—two for each direction (signal and strobe). You can build Transputer networks using the C104 packet-routing switch—a link crossbar for up to 32 T9000 links. A second chip, the C100, interfaces a T9000 link to older Transputer links or serves as a peripheral interface. Accessing peripherals via links offloads the CPU and takes advantage of the 100-Mbps serial lines.

SGS-Thomson 32-bit T9000 Transputer

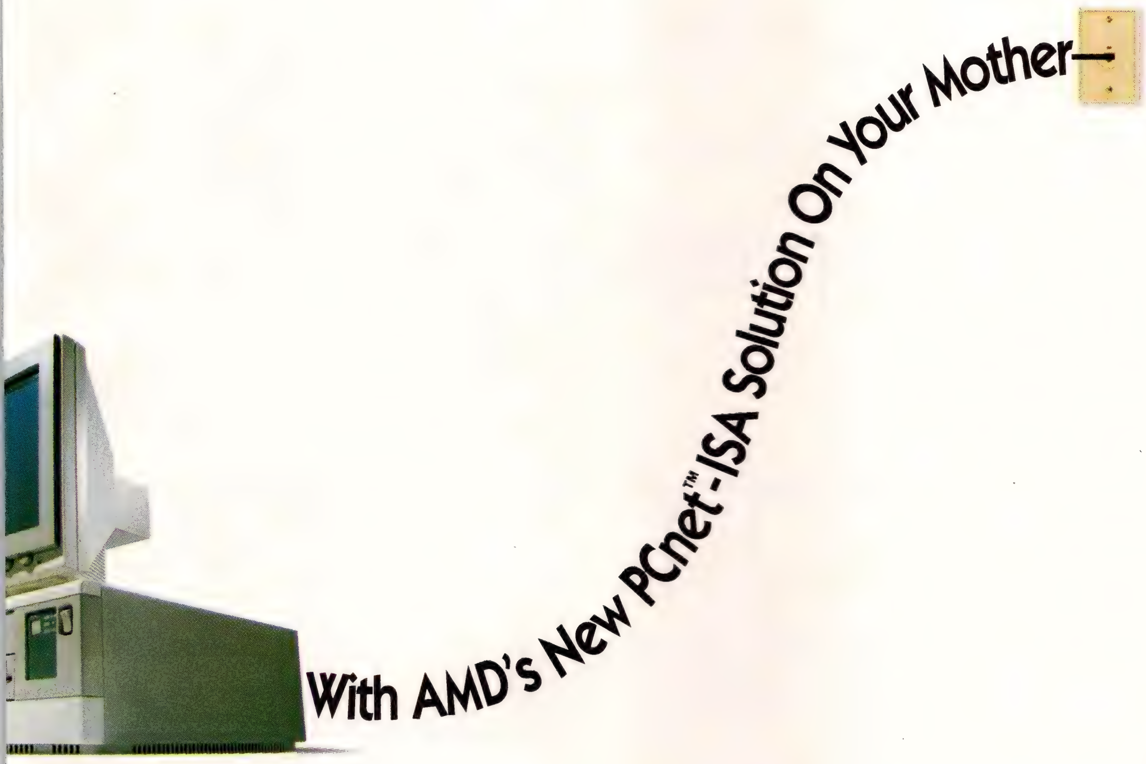
- 40-, 50-MHz clock (5-MHz PLL)
- 3M transistors (0.8 μm)
- 3-register stack
- Superscalar—issues up to 8 instr/cycle
- 5-stage pipeline
- 200 native MIPS peak (25 Mflops)
- Variable-length instructions, most 1 byte
- Microprogrammed CPU scheduler
- On-chip 64-bit FPU
- 64-byte workspace cache
- 16-kbyte fully associative cache; up to 4 simultaneous accesses per cycle
- 4×32-bit crossbar data path
- Virtual-channel communications processor manages 4 100-Mbps virtual serial links and 2 serial control links
- 8-, 16-, 32-, 64-bit memory interface (multiplexed)
- 3V; 208-lead ceramic leadless chip carrier
- $450 (1000)



The T9000 Transputer combines a superscalar, stack-oriented CPU with four high-speed serial links for peripherals and multiprocessing. The CPU incorporates a microcoded operating-system scheduler and a communications processor.

ANSI C and C++ compilers are available for the Transputer and the T9000. These compilers let you easily write code to execute on one or more Transputers. The number of processors is transparent to the code, and the code is partitioned into processes that communicate with each other via virtual channels. These processes may run on the same or different CPUs. The C and C++ compilers eliminate the adoption problems that plagued the early Transputers: Initially, the μP was designed to run with Occum, an advanced parallel-processing language. Unfortunately, Occum was not widely accepted and limited Transputer use accordingly. Occum is still available for the Transputer and has built up a following.

The 16- to 32-bit processors in the Transputer family need minimal ex-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tra logic for embedded-systems applications. The T9000, for example, can directly drive up to 32 Mbytes of memory with no additional logic. Transputers are available as chips, bus-based boards, and CPU-plus-RAM modules.

Development tools include the Inquest PC-based windowing debugger, which lets you debug source code via a control link. SGS-Thomson has also developed Ethernet-gateway drivers that let you debug a Transputer over an Ethernet local network using a PC or Sun-4 workstation.—**Ray Weiss**

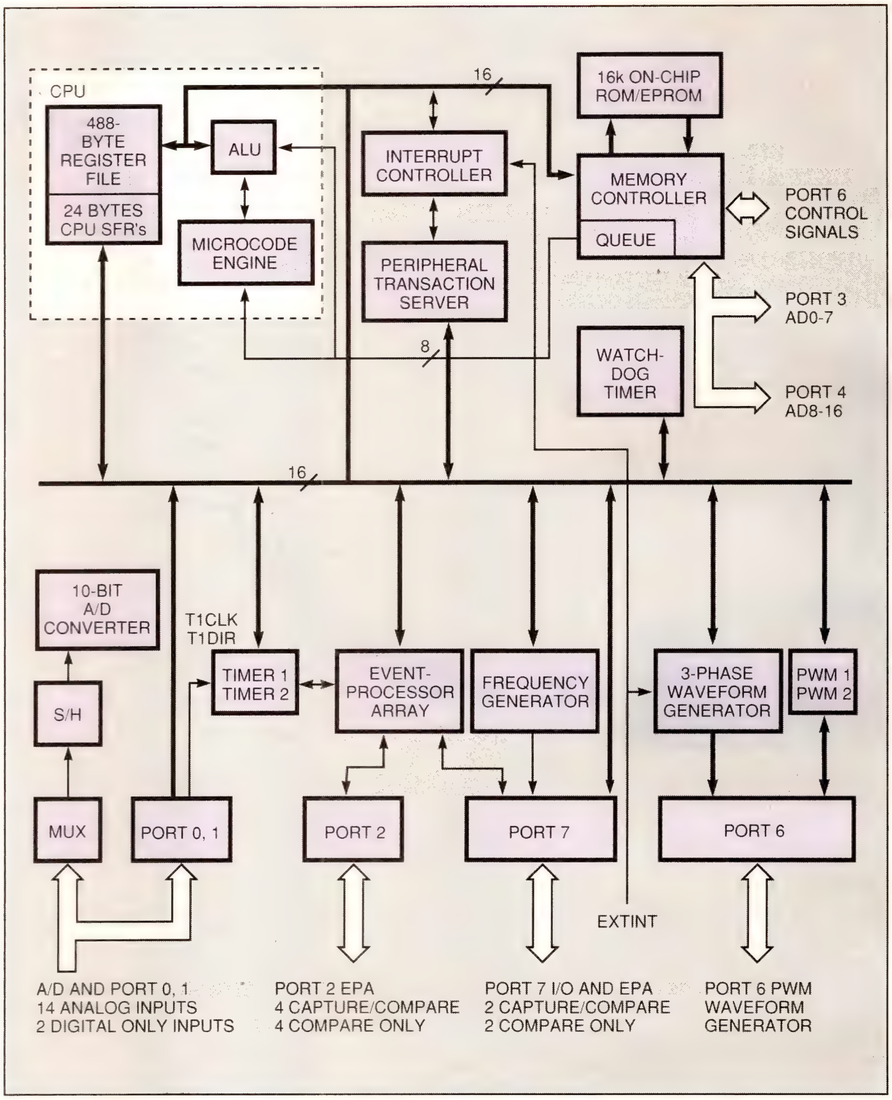
SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6200. FAX (602) 867-6102. **Circle No. 314**

16-bit μC targets remote motor control

Electric motors are a specialized control application, which increasingly demands specialized components. Microcontroller vendors are tailoring their chips to drive costs, as well as design and programming time, down. Intel's 8XC196MD, which integrates a 16-bit μC with specialized motor-control peripherals, is capable of controlling both dc and 3-phase ac induction motors.

Even though the 80C196MC is a pioneering 16-bit μC architecture, it has a modern peripheral set including a timer complex for event monitoring and control, PWMs for motor control, a 3-phase motor controller, a 13-channel A/D converter, and an I/O controller to offload the CPU for event processing.

The 8XC196MD is an extension of the earlier 8XC196MC, which was designed for motor control. Like the 8XC196MC, the 8X196MD peripheral set includes two PWMs for controlling motors by varying the control signal's duty cycle. The PWMs share the same programmable frequency, but you can set the duty cycles for each separately.



The 8XC196MD, which integrates a 16-bit microcontroller with specialized motor-control peripherals, is capable of controlling both dc and 3-phase ac induction motors.

Both versions of the controller have a waveform generator that generates 3-phase PWM signals. The generator controls a 3-phase motor by varying the feeding-voltage duty cycles and providing three control signals, one for each phase line. It generates three complementary, nonoverlapping PWM pulses with resolutions down to either 125-nsec signal edges or 250 nsec to voltage levels.

Frequency is programmable, as are duty cycle and dead times. The chip provides two high-drive outputs for each motor phase. These

Intel 8XC196MD 16-bit μC

- 16 MHz (internal)
- 488-byte register file (serves as data memory, register sets)
- 24-byte special function registers
- 16-kbyte program ROM/OTP
- 1.75-μsec MPY, 3-μsec DIV
- PTS—peripheral controller
- 12-channel, 10-bit ADC
- 2 16-bit timers
- 12-channel event processor array (free timer with capture/compare registers for each channel)
- frequency generator (square wave)
- 3-phase waveform generator
- 3 PWMs
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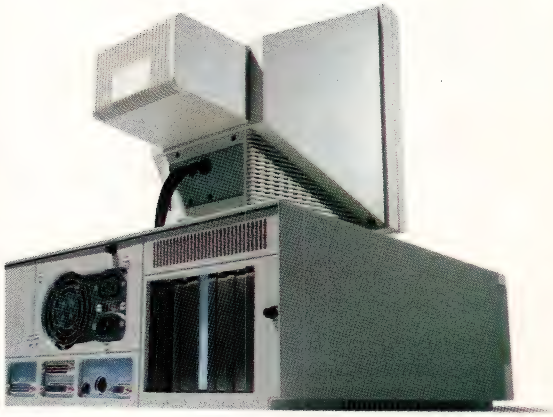

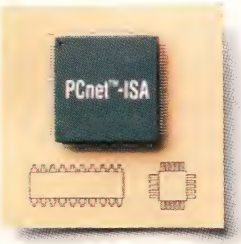

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outputs have programmable polarity. For protection, program an external event to disable drive outputs in response to an error.

Additionally, the new chip has a frequency generator for applications such as infrared communications. This peripheral lets you generate a 50% duty cycle (square wave) with frequencies ranging from 4 kHz to 1 MHz (running at 16 MHz). The generator is controlled via two SFRs (special-function registers) as a memory-mapped peripheral.

The 8XC196MD's A/D converter takes in up to 13 channels and routes them to the converter for 8- or 10-bit conversions. An 8-bit conversion takes 7 μsec. The sample and convert times are programmable, as are threshold detection and offset correction.—**Ray Weiss**

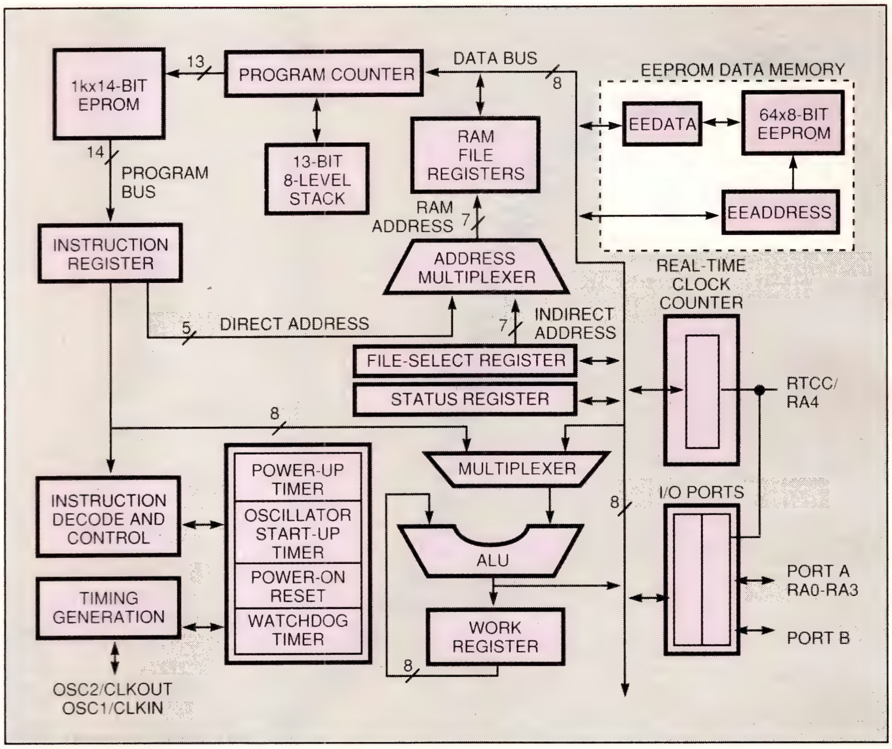
Intel Literature Center, Box 7641, Mount Prospect, IL 60056. Phone (800) 468-8118. **Circle No. 315**

Microchip PIC adds EEPROM data memory

For some embedded applications, RAM and ROM don't cut it. These applications need small chunks of writable, nonvolatile memory to hold critical information. Microchip's PIC 16C84 extends the 8-bit μC architecture by adding 64 bytes of 10-msec write EEPROM data memory.

You can use this EEPROM to store changeable key data, such as security codes, data-input values, and interim data points. You access the EEPROM as a memory-mapped peripheral through the RAM register set. Both EEPROM address and data registers are set for a write; or, the address registers are set for a read. You control operations on the EEPROM via bits set in a hardware-control register.

The EEPROM is perfect for holding slowly changing data, and it provides data at the same read rate as the register file. EEPROM reads take 10 msec; reads take a single CPU cycle (400 nsec at a 10-MHz clock rate). The 16C84 uses a 10-MHz internal clock, which is half the rate of faster PICs.



To hold key data, the PIC 16C84 integrates a 64-byte EEPROM data memory in the low-end 8-bit μC.

As second-generation extensions of the PIC 16C5x 8-bit μC family, the 16C71 and 16C84 μCs have additional interrupts and a wider ROM instruction word. Earlier PICs, with 2-stage execution (200 nsec/cycle, 2 cycles/instruction), lacked interrupt facilities and had a shallow hardware stack facility. The new μCs extend the ROM instruction word from 12 to 14 bits and add Sleep mode; one external and three internal (including wake-up) interrupts; and a deeper stack (from two to eight levels).

Microchip PIC 16C84
8-bit μC

- 10-MHz internal clock (static CPU)
- 2-stage execution (2 cycles)
- 35 single-word instructions
- 36-byte register file
- 1k-word (14-bit-wide) ROM
- 64-byte EEPROM data memory
- 13 I/O pins (to 25-mA sink/pin)
- 1 ext interrupt (8-level stack)
- Real-time clock; watchdog timer
- 2 to 6V (2-mA typ at 5V, 4 MHz)
- In 18-pin DIP or SOIC, $3.72 (10,000)

PIC μCs are popular for low-end embedded applications. Engineers use PIC μCs' fast execution cycle to compensate for a minimal peripheral set. PICs are available with ROM, EPROM, and OTP (one-time-programmable) memory.

Microchip also sells PICMaster-16C, a development system for PIC chips, and the PIC 16C84 μC. The system functions as a real-time ICE (in-circuit emulator), monitoring a CPU probe, emulating ROM memory, and collecting execution trace data. Users run the development tool from an IBM PC under Microsoft Windows. PICMaster-16C sells for $3450.—**Ray Weiss**

Microchip Technology Inc, 2355 W Chandler Blvd, Chandler, AZ 85224. Phone (602) 786-7200. FAX (602) 899-9210. **Circle No. 316**

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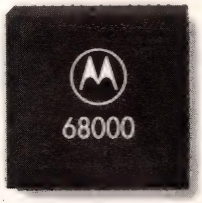

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CIRCLE NO. 161

EDN
Ground-bounce tests
REVISITED

Ground bounce can cause the failure of ICs, intermittent problems in systems, and possibly even the death of a product. It is critical that you evaluate your design to see if ground bounce will affect it. These tests will help you understand the relative noise between various CMOS bus-driver ICs.

David Shear, Technical Editor

Four years ago, EDN tested advanced CMOS logic (ACL) chips to compare their ground bounce (see **box,** "Ground-bounce primer"). At that time, the controversy was over packaging.

In the intervening four years, many new products have become available. We originally tested 11 chips. This time, we tested 72. Instead of just two package types, end-pin and center-pin DIP, we tested nine package types. We only tested octal parts. Wider bus parts, just becoming available, were not tested for this article.

Grounds will always bounce. It is not possible to eliminate this noise source completely. But the device-induced ground bounce has decreased for many of the logic families. Additional circuitry, limiting output swings, using bipolar output stages, gradually turning on the output transistors, and new packaging have all reduced ground bounce (**Ref 1**).

What managers need to know

- Ground bounce is still a problem
- Design changes in some bus-driver ICs have reduced ground bounce
- Smaller packages result in less ground bounce
- Simulation is the best way to evaluate ground bounce in a specific application—if you use good models

There are many factors to consider when selecting a logic family. In some cases, ground bounce may be the deciding factor. In other cases, it may not even be a consideration. Cost, power consumption, operating temperature, drive capability, output skew, radiation hardness, or how much you like the salesperson may be the major criterion.

In this article, we only look at ground bounce, propagation delay, and transition time on one test fixture, at one voltage, and at room temperature. This allows a compari-

New packaging techniques keep ground bounce at low levels in many applications. (Photo courtesy National Semiconductor Corp)

son between devices *under these conditions.*

It is not possible to provide a single number defining the ground bounce of a family. Don't look at our results and amplify small differences in ground bounce into major influences on your purchasing decision.

The test results for the DIPs are shown in **Figs 1** and **2**, as well as in the scope photos starting on page 129. DIPs were chosen as the worst case, because in all but one case, the DIP had the highest ground bounce. Other packages were smaller and had lower lead inductance, which resulted in a lower V_{OLP} (voltage output low pulse, the worst case number for ground bounce). The test results for the other package types are included on the scope-photo pages. (Note: National Semiconductor's ABT family is not available in DIPs)

Ground bounce is dependent upon the speed of the device, *so it's important to include the speed of the device when referring to ground bounce.* A slower device from the same manufacturer will have a lower V_{OLP} than a faster device. Propagation delay (t_P) is a good indication of the speed of the device. **Fig 1** shows the value of $V_{OLP\text{-}HL}$ vs t_{PHL} (refer to **Table 1** for naming conventions).

Fig 2 shows another way of looking at the results. This figure plots a speed-noise product vs transition time for the DIPs. The speed-noise product is obtained by multiplying the V_{OLP-HL} and the t_{PHL}. It is plotted against the fall time (t_f).

You can see that the different families are grouped together on both of these plots. The BiCMOS parts had the lowest V_{OLP-HL} (0.3 to 0.7V) and the lowest speed-noise product (1.2 to 3.5V-nsec). The center-pin parts and the newer ACL parts with reduced output voltage, controlled turn on, and other improvements had a V_{OLP-HL} from 1.0 to 1.5V and a speed-noise product of 5 to 7.5V-nsec. The older ACL devices had a V_{OLP-HL} between 1.9 and 3V.

Our tests suggest (see **box,** "The test fixtures and methods"):

- The BiCMOS parts are quietest
- The new ACL parts are quiet (V_{OLP-HL} is less than the static TTL threshold, 1.5V)
- The older ACL parts are noisiest.

For noise-sensitive applications, you will have a harder time using the older ACL parts, but that does not mean you can't use them. You will just have to exercise a bit more care than with the quieter parts.

The devices with built-in series resistors had lower V_{OLP} than the same devices without the resistors. Placing a resistor in series with the output is often used to control the output and reduce ground bounce. The 2XXX series devices merely place these resistors inside the package. The 2XXX devices tested are included with the scope photo of the same part without the resistor.

Fig 3 shows the results for the 3.3V devices. We tested SOIC versions of the 3.3V devices because few DIP versions were available. We used the same test procedures as with the 5V parts, except that the V_{CC} was 3.3V. The reduced V_{CC} lowered the ground bounce.

One of the promises companies made in 1989 was that smaller packages would have lower lead inductance, resulting in lower ground bounce. We verified the lower lead inductance by using the Tektronix Interconnect Parameter Analyzer (IPA 310). We found the ground-lead inductance on a DIP, SOIC, QSOP, and TSSOP to be 6.7, 4.5, 3.5, and 2.2 nH, respectively.

The ground bounce measured on the smaller packages was usually less than that on the DIP, but not

Ground-bounce primer

Ground bounce, also known as simultaneous switching noise, occurs when an output of a logic device changes state (**Fig A**). A chip resides in a package that has some amount of lead inductance on the V_{CC} pin, the output pin, and the ground pin. When the chip's output changes state, the charge remaining in C_L is drained through the lead inductance on the output lead and the ground lead.

The changing current flowing through the inductance to ground induces voltage V_{GB}. This voltage is the ground bounce. The internal ground is then elevated from system ground, causing the chip in the package to have a different ground than the rest of the system. If the ground bounces high enough, logic thresholds can be exceeded, causing false logic transitions.

Also, when an output bounces below ground, a negative voltage is fed to whatever the output is driving. This negative voltage may be large enough to damage the input of the IC being driven.

A worst-case condition exists when many outputs are changing state at the same time. The current to drain each of the load capacitances adds together. The total current flows through the ground lead. The ground bounce that occurs when many outputs switch simultaneously is what we measured for this article.

Note that the board inductance in **Fig A** is also in the ground path. Even if the package inductance was reduced to 0, you still have to make sure that the board inductance is low enough not to cause the ground to bounce anyway.

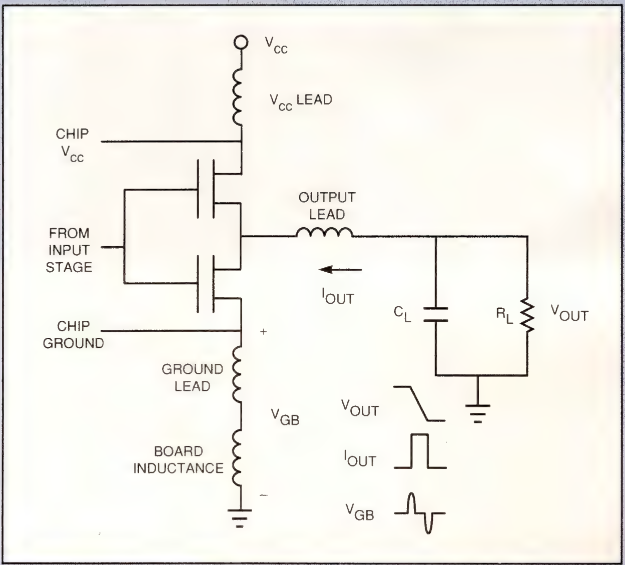


Fig A—The inductance between the chip ground and the system ground is the major contributor to ground bounce. The changing current flowing through this inductance induces voltage V_{GB}, shifting the chip's ground. Note that the test fixtures used in this test have a very low board inductance. You have to make sure that the board inductance in your design is also low.

as much less as the reduced inductance would indicate. Over the years, predictions of ground-bounce reduction have varied from a linear relationship, to a reduction proportional to the square root of the lead inductance, to a maximum reduction of 25% no matter how much the lead inductance was reduced.

We determined the reduction in ground-bounce due to the package by comparing the $V_{OLP\text{-}HL}$ of each 20-pin package type to the $V_{OLP\text{-}HL}$ of the DIP. We found the reduction due to the package to be 17% for the SOIC, 15% for the QSOP, 24% for the SSOP, and 26% for the TSSOP.

This data seems to support the view that the most the package can reduce $V_{OLP\text{-}HL}$ is about 25%. A possible explanation is that as the package inductance decreases, the device runs faster and the di/dt goes up. This adds some V_{OLP} to the reduction, countering the $V_{OLP\text{-}HL}$ reduction due to lower package inductance.

All test fixtures are not equal

The QSOP test fixture masked some of the advantages of that package. All other fixtures were made by ESH Inc (Tempe, AZ) and assembled by Texas Instruments (TI). They had similar characteristics. The QSOP fixture was made by National Semiconductor and included extra traces and switches for other tests. These extra components

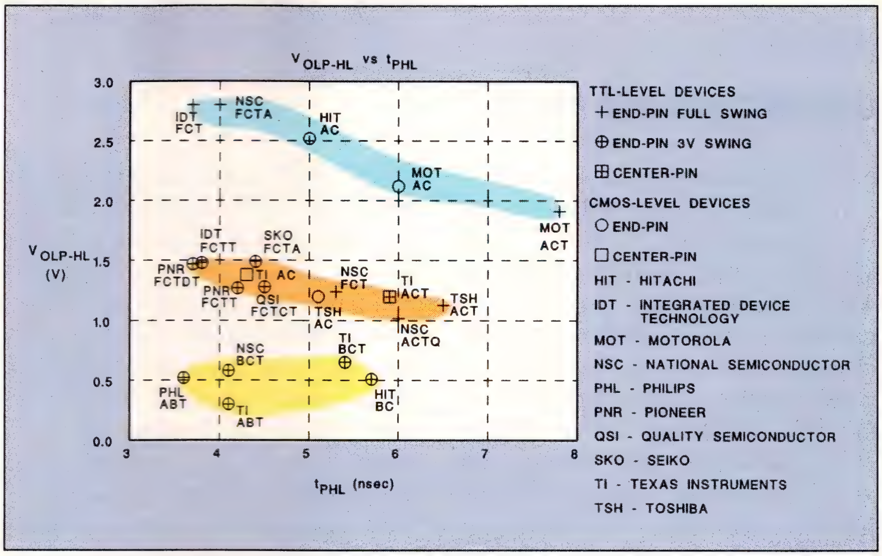


Fig 1—When referring to ground bounce, make sure you also reference the speed of the device. Propagation delay is a good representation of speed. Here the ground bounce ($V_{OLP\text{-}HL}$) is shown vs the propagation delay (t_{PHL}) for dual-in-line packages.

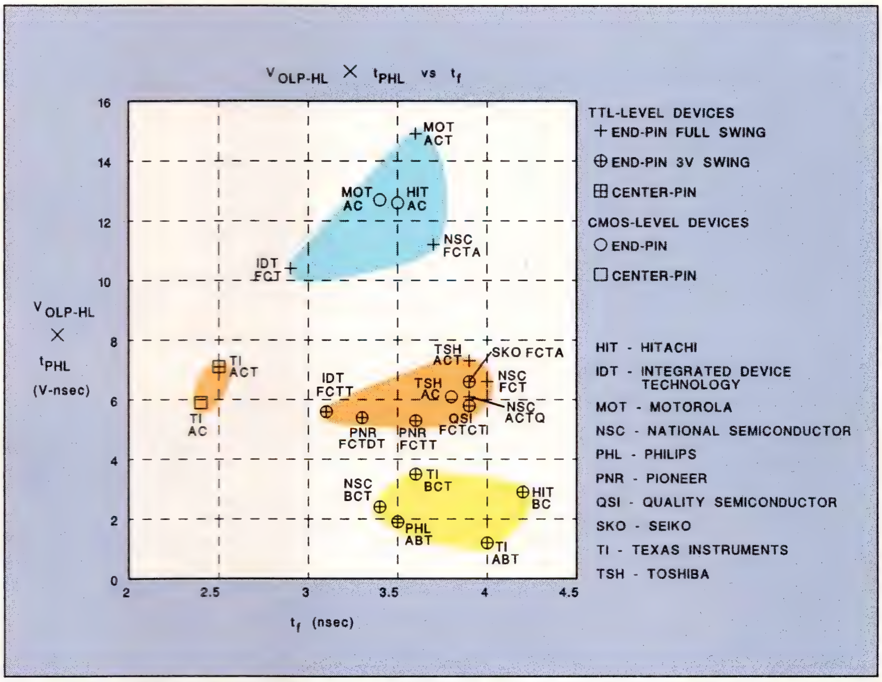


Fig 2—The speed-noise product is a product of the ground bounce and the propagation delay. We've plotted the speed-noise product vs the fall time (t_f) for dual-in-line packages.

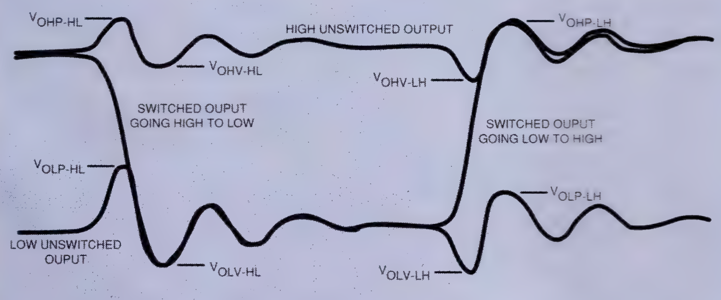


Table 1—Naming conventions

V_{OLP} =Voltage output low peak
V_{OLV} =Voltage output low valley
V_{OHP} =Voltage output high peak
V_{OHV} =Voltage output high valley
-HL=When output is going from high to low
-LH=When output is going from low to high

In order to clarify the peaks and valleys in the complex ground-bounce waveforms, these naming conventions were used in this article.

may have influenced the results.

It might have been better to test the V_{OLP} reduction due to the package by taking die from the same wafer and putting it into different packages, which would remove device variations. But the relatively tight grouping within the various families suggests that the variations between parts aren't that great. There was one case of a major variation between different lots: The Quality Semiconductor QS74FCT244CTQ (QSOP) had a $V_{OLP\text{-}HL}$ 35% higher than the same device in a DIP. The company claims this result is anomalous. We sent a copy of the data to the manufacturers that participated in this test and asked them to check any numbers that seemed out of line. Quality Semiconductor was the only company that had a problem with the data and suspected our test fixture or methods, because they had never seen a $V_{OLP\text{-}HL}$ this high from any of its parts in any package.

We retested the part and found no error. The company tested a device from the same lot and found numbers similar to ours. According to Mark Muegge, Senior Applications Engineer at Quality Semiconductor, an internal mixup caused nonproduction parts to get into the production parts stock. Our samples were pulled from this stock. QSI claims that this lot is not within production standards. The parts are much too fast, and the company has purged its stock of these parts. QSI also stated that it is changing its procedures to make sure this does not happen again.

When reviewing any of the results, remember that this data was taken using test conditions. Keep in mind that

The test fixtures and methods

To conduct a test that compared all of the parts as accurately and fairly as possible, we interviewed engineers at the IC manufacturers' characterization labs. By viewing the test equipment, the test fixtures, and the methods used, we determined that most manufacturers were using similar fixtures and methods.

We set up a similar lab. The parts tested were supplied by the manufacturers. To be included in the article, the manufacturer had to have a 244-type octal buffer in production by January 1, 1993; the part had to be available through distribution; and the samples had to be randomly selected.

Texas Instruments assembled the test fixtures using boards manufactured by ESH Inc (Tempe, AZ), National Semiconductor provided the QSOP test fixture. **Fig A** shows a typical channel. The input is terminated with 50Ω (56Ω in parallel with 450Ω + 50Ω). The output is loaded with 50 pF in parallel with 500Ω (450Ω plus a 50Ω termination or a scope's 50Ω input).

The DIP test fixture was the same one used in EDN's 1989 ground-bounce tests (**Ref 2**). It is the only one that uses sockets (very small low-inductance ones) and buses all seven inputs together.

All other test fixtures are for surface-mount packages and have gold contacts on the boards and plastic clamps to hold the chip leads to the board. The inputs were not bused together on these boards. A separate data time-generator channel supplied a signal to each input.

In all cases, the static inputs were driven by the data time generator. Even the enable inputs, which must be low to enable the outputs, were driven by the generator. It was important that these inputs not be shorted directly to ground. If they were, some of the ground current could leave the chip through these pins and lower the measured V_{OLP} by about 200 mV.

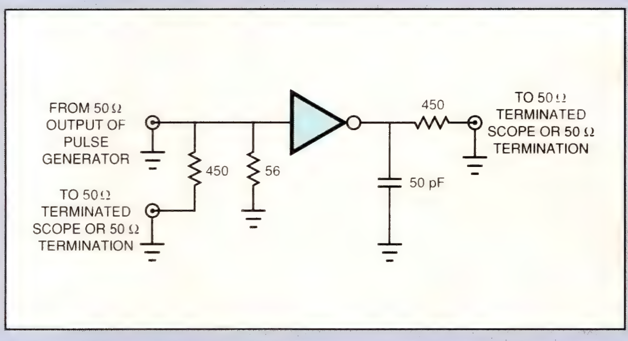


Fig A—All of the components on the test fixtures are surface-mount devices placed very close to the device under test.

Fig B shows how we connected the instruments to the fixture. The temperature was between 21 and 22°C. V_{CC} was either 5.0 or 3.3V.

We set the data time generator for a transition time of 2.5 nsec. The actual transition time varied depending on the device being driven. Refer to the scope photos starting on pg 129 for transition-time data.

When testing TTL parts, the input signal was 0 to 3V and all timing measurements used a threshold of 1.5V. For CMOS parts, the input signal was 1 to 4V and the timing threshold was 2.5V. The pulse rate was 1 MHz. Output skew was less than 100 psec. Transition times were measured from 10 to 90% of full logic swing.

The signal is taken to the scope via a 50Ω cable. The 450Ω resistor and the 50Ω termination in the scope create a robust and repeatable divide-by-ten probe built onto the test fixture. Handheld probes can greatly affect the measured results.

The data time generator was a Tektronix HPS9003.

- All data was taken with seven outputs switching
- V_{CC} was 5.0 or 3.3V
- The temperature was 21 to 22°C
- The load on each output was 50 pF and 500Ω.

Our test results don't necessarily indicate how these parts will work in your design because the amount of ground bounce that your application can tolerate is difficult to determine. All logic inputs have a variable threshold (**Fig 4**). When a signal exceeds the static threshold, the output will change state. But if a signal on the input exceeds the

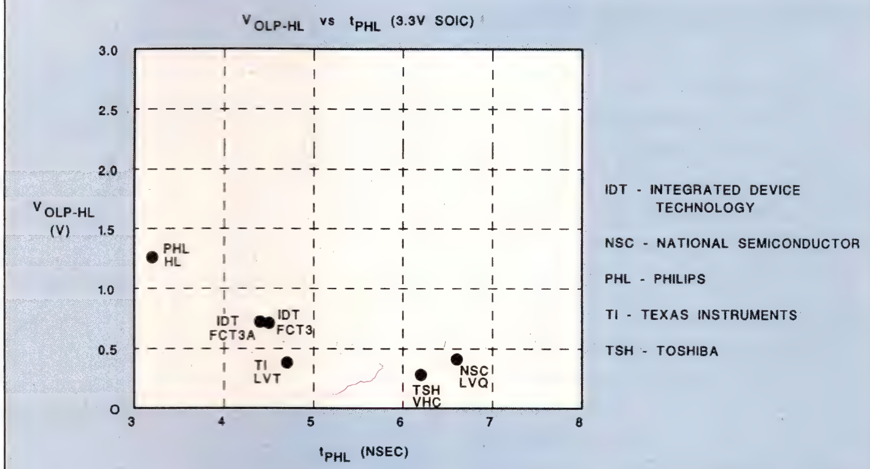
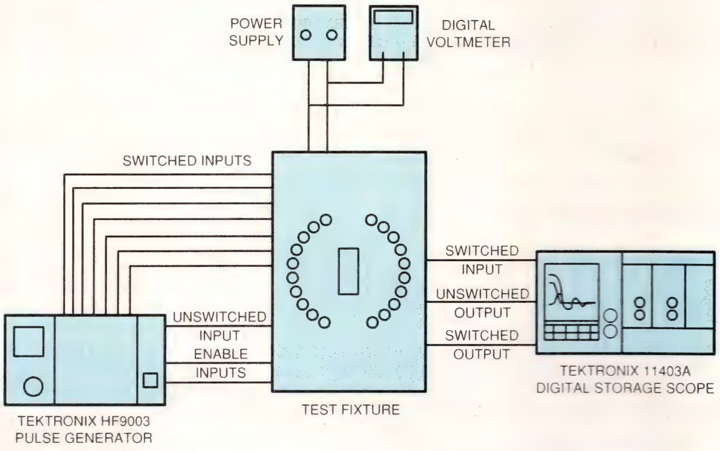


Fig 3—Few 3.3V devices come in DIPs, so we tested the SOICs. Here we've plotted the ground bounce ($V_{OLP\text{-}HL}$) of the 3.3V logic vs the propagation delay (t_{PHL}).



	20-pin device	24-pin device
Switched inputs	4, 6, 8, 11, 13, 15, 17	14, 15, 16, 17, 20, 21, 23
Switched output measured	16	10
Unswitched input	2	22
Unswitched output	18	2
Enables	1, 19	13, 24
V_{CC}	20	18, 19
Ground	10	5, 6, 7, 8

Fig B—The data time generator created the switched signals as well as the static signals. Note that traditional scope probes are not used. Divide by ten probes are built into the test fixture.

The digital-storage oscilloscope (DSO) was a 1-GHz-bandwidth Tektronix 11403A. The cables were 48-in. RG-316 coax with SMB connectors on one end and either SMA (to data time generator) or BNC connectors (to scope) on the other end.

We used the following procedure to gather the data presented in this article:

1. Put DUT in test fixture
2. Apply power
3. Check voltage on power supply
4. Turn on data time generator outputs
5. Check voltage on power supply
6. Recall FPS 1 (FPS 3 for CMOS)
7. Set unswitched input low
8. Check all seven outputs switching
9. Record $V_{OLP\text{-}HL}$, t_{PHL}, t_f
10. Set unswitched input high
11. Record $V_{OHV\text{-}HL}$
12. Recall FPS 2 (FPS 4 for CMOS)
13. Set unswitched input low
14. Record $V_{OLP\text{-}LH}$, t_{PLH}, t_r
15. Set unswitched input high
16. Record $V_{OHV\text{-}LH}$
17. Check voltage on power supply
18. Turn off data time generator outputs
19. Turn off power
20. Remove DUT

All measurements were made with the automated features of the DSO. The four FPSs (front panel settings) set the trigger slope and measurement parameters.

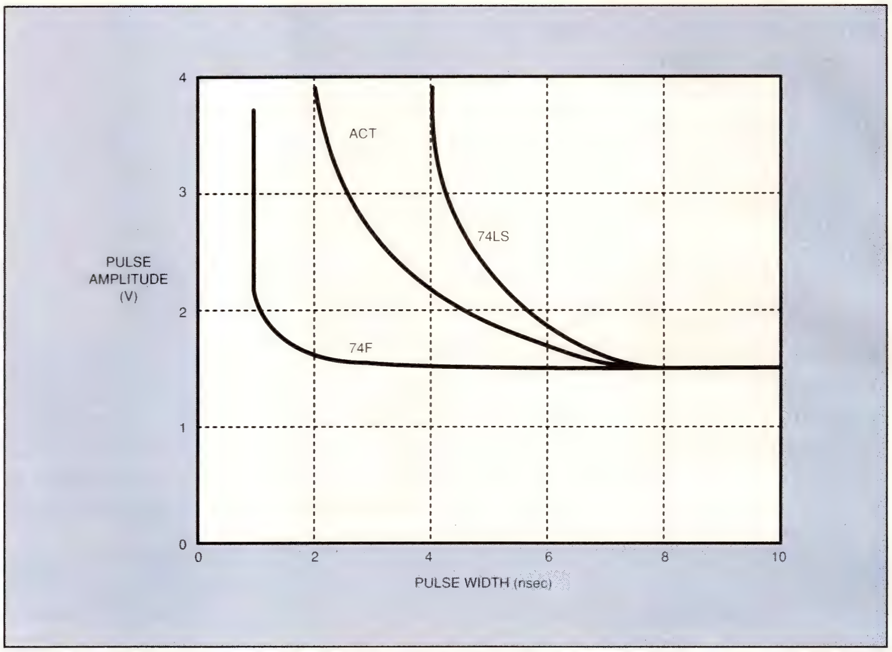


Fig 4—The dynamic threshold of different logic families shows that as the input pulse width gets shorter, the voltage must get higher to affect the output of the device.

static threshold for a very short time, the output will not have enough time to react. As the pulse width gets shorter, the input must reach a higher voltage before the output will begin to react.

You must decide how much ground bounce you can tolerate when you are designing your system. If you know what your loads will be, you can run your own tests with that load. If you are planning to drive a terminated transmission line, you should use the transmission-line impedance as a test load.

Simulate your application

Creating test fixtures for specific applications is time-consuming and expensive. Simulation may offer a better approach, if you can get accurate models. It is easy to create models of anything, and any model will give you a result. The difficulty is in making an accurate model.

The output stages of ACL bus drivers are very complex to model. They have evolved far beyond just an output transistor. For example, the ACTQ family from National Semiconductor has a split ground bus and leadframe, graduated output turn on, and undershoot correction circuitry. All of these features will affect the noise of the device

Manufacturers of bus-driver ICs

For more information on bus-driver ICs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

Hitachi America Ltd
Semiconductor & IC Div
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Mail Station #080
Brisbane, CA 94005
(800) 448-2244
Circle No. 301

Integrated Device Technology Inc
2975 Stender Way
Santa Clara, CA 95054-3090
(800) 345-7015
FAX (408) 492-8674
Circle No. 302

Meta-Software Inc
1300 White Oaks Rd
Campbell, CA 95008
(408) 371-5100
(800) 346-5953
FAX (408) 371-5638
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Motorola Inc
Logic IC Div
2200 W Broadway Rd
Mesa, AZ 85202
(602) 962-2908
FAX (602) 898-5020
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National Semiconductor Corp
333 Western Ave
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(207) 775-8755
FAX (207) 775-8745
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Philips Components
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Sunnyvale, CA 94088
(408) 991-2725
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2343 Bering Dr
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Tektronix Inc
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and the complexity of the model.

You also need an accurate model of the packages, the board, the connectors, and any other devices that can contribute to the noise of your system. Once you have models you can trust, you should be able to compare logic families in view of your application.

Many companies are addressing the need for accurate models. Meta-Software, maker of HSpice-circuit simulation tools, has proposed an alliance of IC manufacturers, simulation companies, and model developers called the Meta Signal Integrity Alliance (MSIA). The group's goal is to make accurate models available for simulating ground bounce and other noise conditions.

Philips is taking an active role in creating models. It has produced the *Spice Simulation Design Guide* to help characterize its logic families. Other manufacturers are also working on models.

Tektronix is also helping out with a system called the IPA 310 that uses time-domain reflectometry to measure the characteristics of packages, connectors, and traces—basically anything a signal goes through. The IPA 310 ($74,950) then creates the Spice model that you can use in your simulation.

Ground bounce within the bus-driver IC is getting more manageable but the offending currents still exist. These currents still flow from the chip into your board. Make sure your board can handle them.

References

1. Quinnell, Richard, "Bus-driver ICs," *EDN*, February 3, 1992, pg 78.
2. Shear, David, "EDN's advanced CMOS logic ground-bounce tests," *EDN*, March 2, 1989, pg 88.

Acknowledgment

Many people contributed time and materials to this article. As usual, the complete list is much too long to include here. But I would like to extend special thanks to Sue Foley and Bozidar Janko of Tektronix, Arthur George, Chris Haga, and Mike Thurston of Texas Instruments, Mike Stevens of Philips, and Bill Hall, Jeff Jones, and Raymond Beahm of National Semiconductor.

Author's biography

David Shear is a technical editor for EDN. You can reach him at (503) 754-9310.

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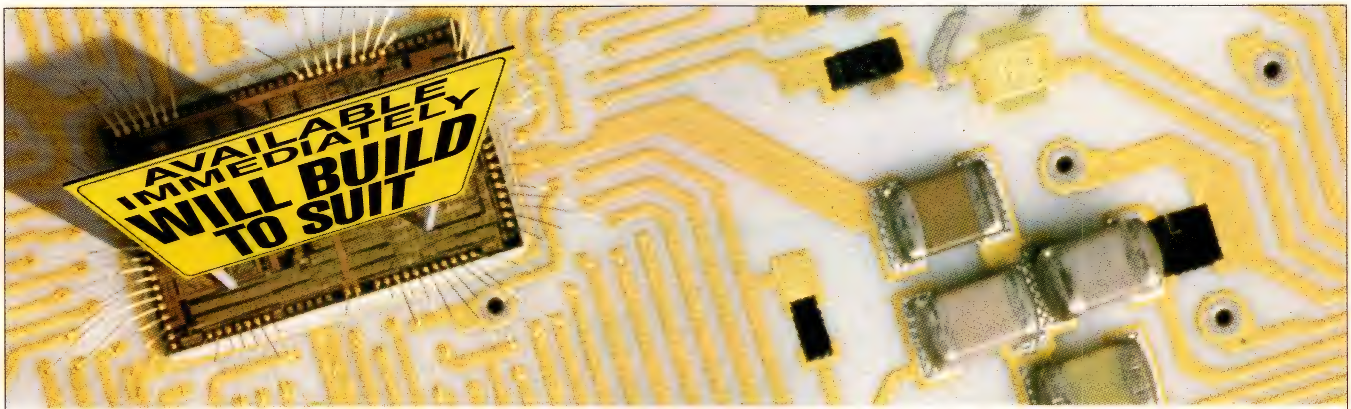
Article continued on pg 129



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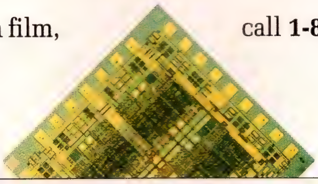

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QS7224	4K x 9	66MHz Clocked Interface

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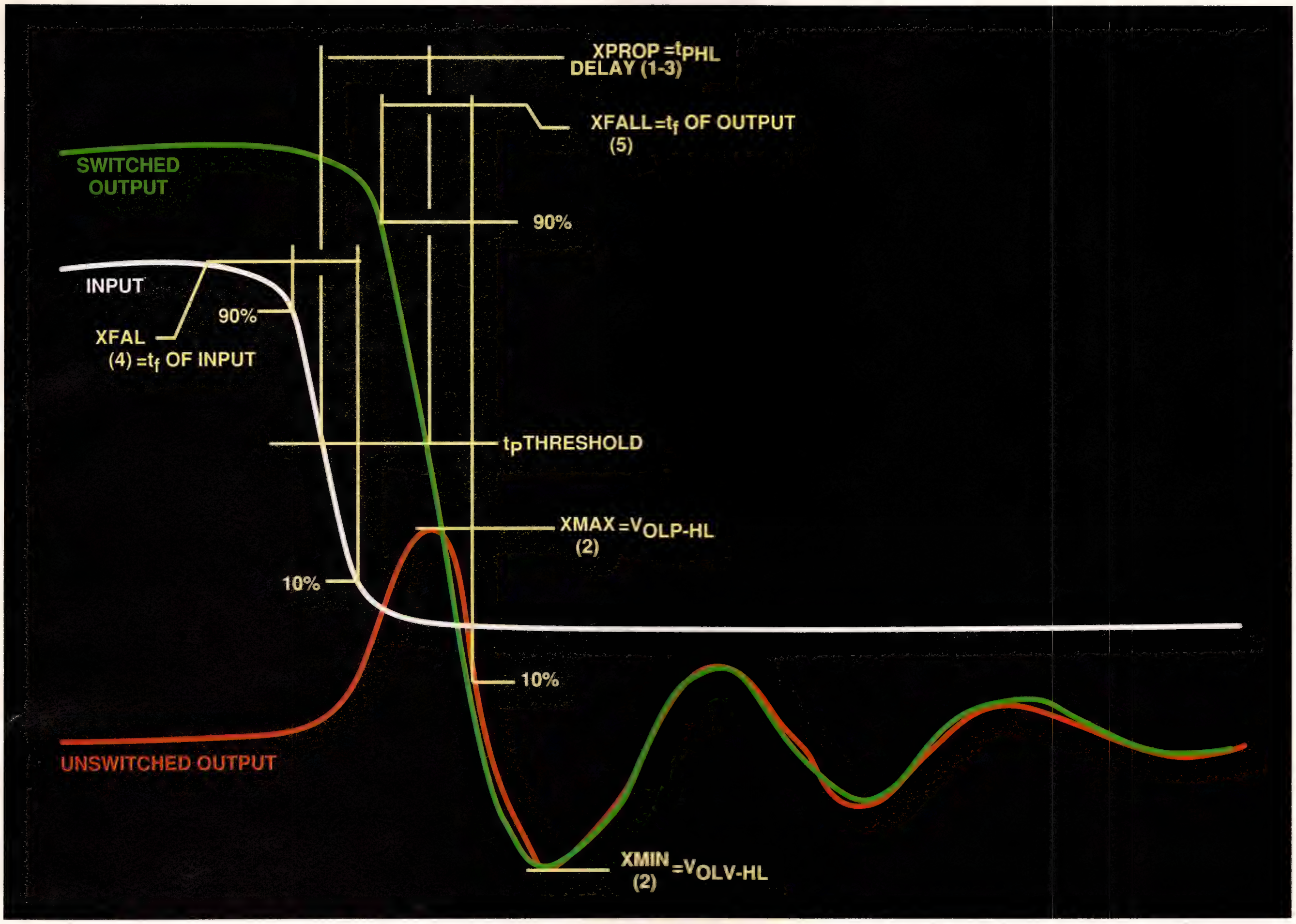


The 11403A digital storage scope's measurements are displayed on the bottom of the scope photo and correspond to these measurements.

3.3V Devices

DEVICE

	Integrated Device Technologies				National Semiconductor		
	74FCT3244P	74FCT3244SO	74FCT3244ASO	74FCT3244PY	74LVQ244SC	74LVQ244QSC	74VHC244MSCX
V_{OLP-HL} (V)	0.90	0.71	0.72	0.68	0.41	0.39	0.20
V_{OLP-LH} (V)	0.77	0.72	0.72	0.64	0.30	0.21	0.07
V_{OHV-HL} (V)	2.66	2.63	2.62	2.64	2.69	2.83	2.66
V_{OHV-LH} (V)	2.45	2.49	2.48	2.54	2.62	2.62	2.69
t_{PHL} (nsec)	4.5	4.5	4.4	4.6	6.6	6.4	6.4
t_{PLH} (nsec)	4.9	4.3	4.3	4.2	6.8	6.6	8.1
t_r (nsec)	4.7	4.2	4.3	3.9	5.3	5.8	8.2
t_f (nsec)	3.8	3.7	3.6	4.1	4.7	5.2	5.9
$V_{OLP-HL}{}^{*}t_{PHL}$	4.1	3.2	3.2	3.1	2.7	2.5	1.3
FIXTURE	DIP	SOIC	SOIC	SSOP	SOIC	QSOP	TSSOP

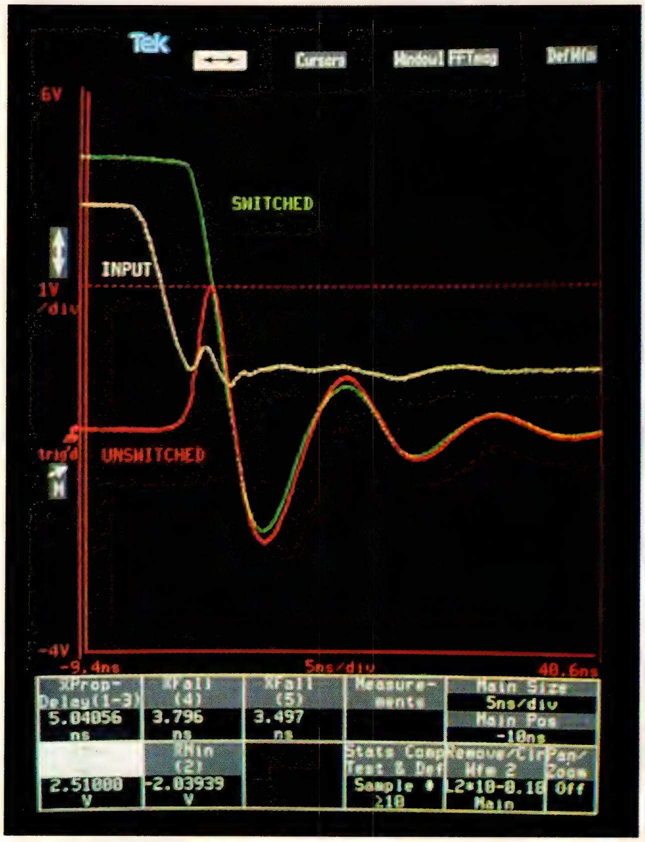
3.3V Devices

DEVICE

	National Semiconductor	Philips	Texas Instruments		Toshiba	
	74VHC244MSCX (5V)	74HL33244D 3.3V	SN74LVT244DW 3.3V	SN74LVT244PWLE 3.3	TC74VHC244FW 3.3	TC74VHC244FS 3.3
V_{OLP-HL} (V)	0.55	1.26	0.38	0.33	0.28	0.22
V_{OLP-LH} (V)	0.20	0.23	0.31	0.30	0.10	0.08
V_{OHV-HL} (V)	4.19	2.42	2.74	2.75	2.70	2.67
V_{OHV-LH} (V)	4.07	1.60	2.28	2.34	2.68	2.68
t_{PHL} (nsec)	5.2	3.2	4.7	4.4	6.2	6.2
t_{PLH} (nsec)	6.4	3.7	3.9	3.8	7.4	7.7
t_r (nsec)	5.9	2.9	4.2	4.3	6.8	7.8
t_f (nsec)	4.6	2.3	4.0	3.5	5.8	5.7
$V_{OLP-HL}{}^{*}t_{PHL}$	2.9	4.0	1.8	1.5	1.7	1.4
FIXTURE	TSSOP	SOIC	SOIC	TSSOP	SOIC	TSSOP

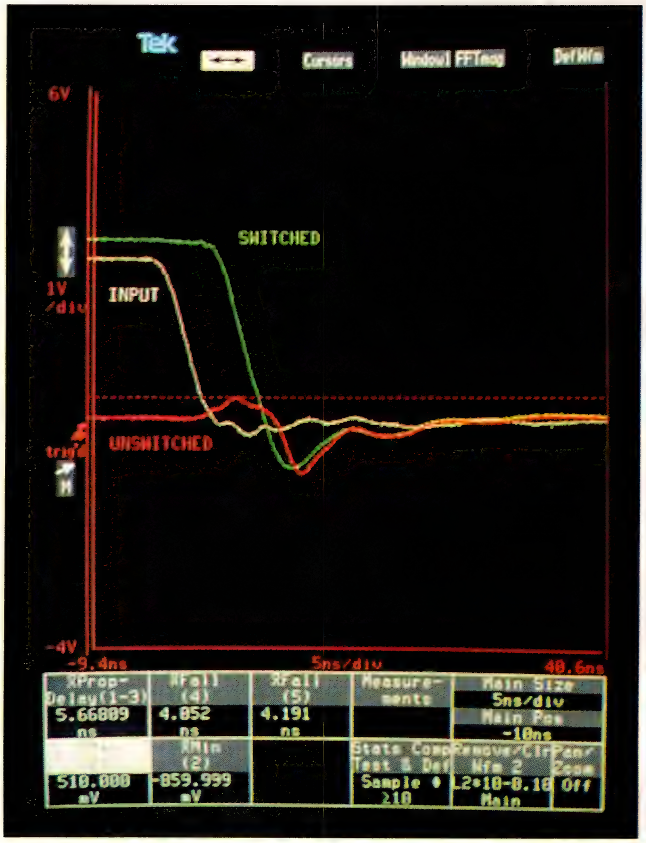
Hitachi AC

	DEVICE
	HD74AC244P
$V_{OLP\text{-}HL}$ (V)	2.52
$V_{OLP\text{-}LH}$ (V)	1.05
$V_{OHV\text{-}HL}$ (V)	4.21
$V_{OHV\text{-}LH}$ (V)	3.31
t_{PHL} (nsec)	5.0
t_{PLH} (nsec)	5.4
t_r (nsec)	4.0
t_f (nsec)	3.5
$V_{OLP\text{-}HL}{}^*t_{PHL}$	12.6
FIXTURE	DIP



Hitachi BC

	DEVICE
	HD74BC244P
$V_{OLP\text{-}HL}$ (V)	0.51
$V_{OLP\text{-}LH}$ (V)	0.47
$V_{OHV\text{-}HL}$ (V)	3.06
$V_{OHV\text{-}LH}$ (V)	2.87
t_{PHL} (nsec)	5.7
t_{PLH} (nsec)	6.4
t_r (nsec)	5.1
t_f (nsec)	4.2
$V_{OLP\text{-}HL}{}^*t_{PHL}$	2.9
FIXTURE	DIP



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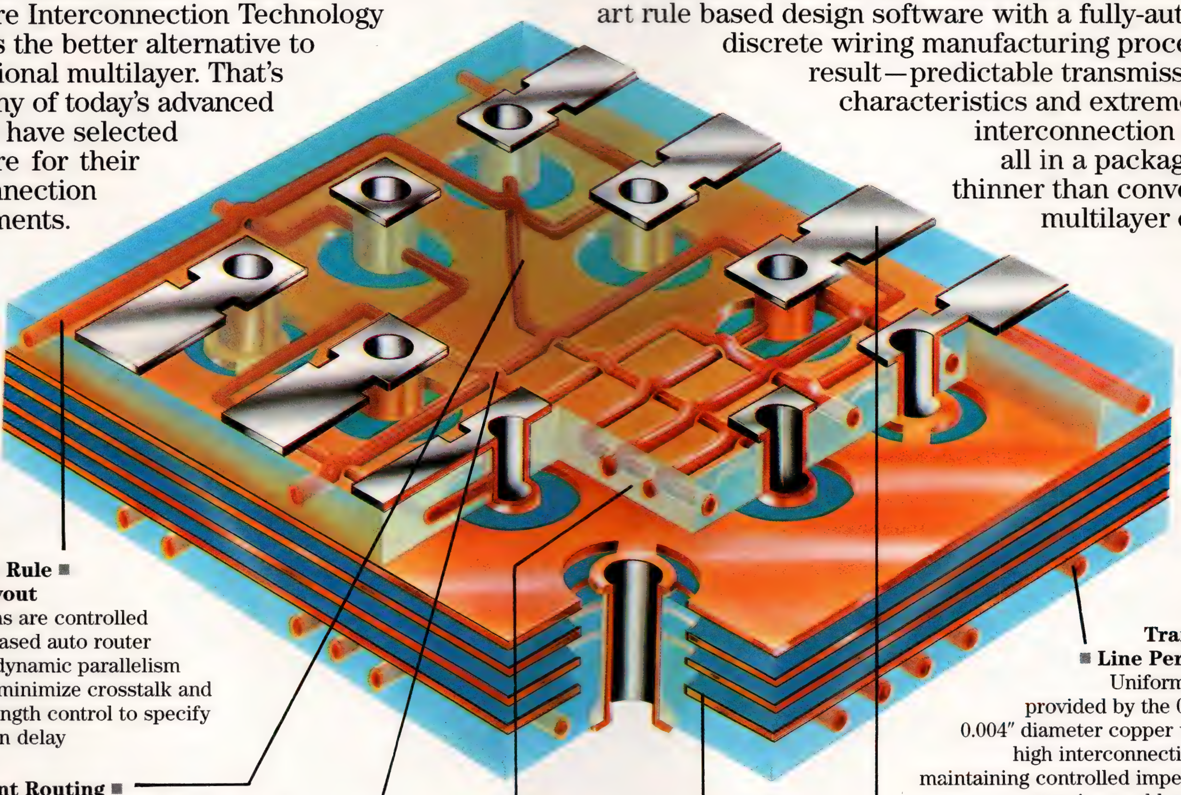
When you need superior performance in a circuit board that's smaller...denser...faster... Multiwire Interconnection Technology provides the better alternative to conventional multilayer. That's why many of today's advanced systems have selected Multiwire for their interconnection requirements.

Multiwire Technology is more than just a circuit board. It's an advanced interconnect system, integrating state-of-the-art rule based design software with a fully-automated discrete wiring manufacturing process. The result—predictable transmission line characteristics and extremely high interconnection density, all in a package much thinner than conventional multilayer circuits.



Electrical Rule Based Layout ▪
Signal paths are controlled by a rule based auto router providing dynamic parallelism control to minimize crosstalk and dynamic length control to specify propagation delay

Concurrent Routing ▪
Signal paths can be routed in both X, Y and 45 degrees on a single wiring layer, achieving extremely high density wiring allowing up to 4 wires to pass between holes on 0.050″ centers

No Via Holes ▪
Polyimide insulated wire allows conductors to cross on a single layer, eliminating the electrical discontinuity associated with interstitial via holes required by conventional multilayer circuits

Superior Thermal Performance ▪
Extremely thin interconnect layer minimizes thermal resistance to the internal copper planes or optional metal core

▪ **Transmission Line Performance**
Uniform geometry provided by the 0.0025″ and 0.004″ diameter copper wire offers high interconnection density, maintaining controlled impedance, low attenuation, and low crosstalk

▪ **High Density Surface Mounts**
Electroplated copper pads compatible with both high density SMT and through hole components

▪ **Multilayer Power And Ground**
Discrete copper planes provide low impedance power and ground distribution essential for high speed digital systems

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Lisses, France
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PACIFIC RIM

Hitachi Chemical Company, Ltd.
Tokyo, Japan
81-3-3346-3111 ▪ FAX 81-3-3346-3475

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CIRCLE NO. 80

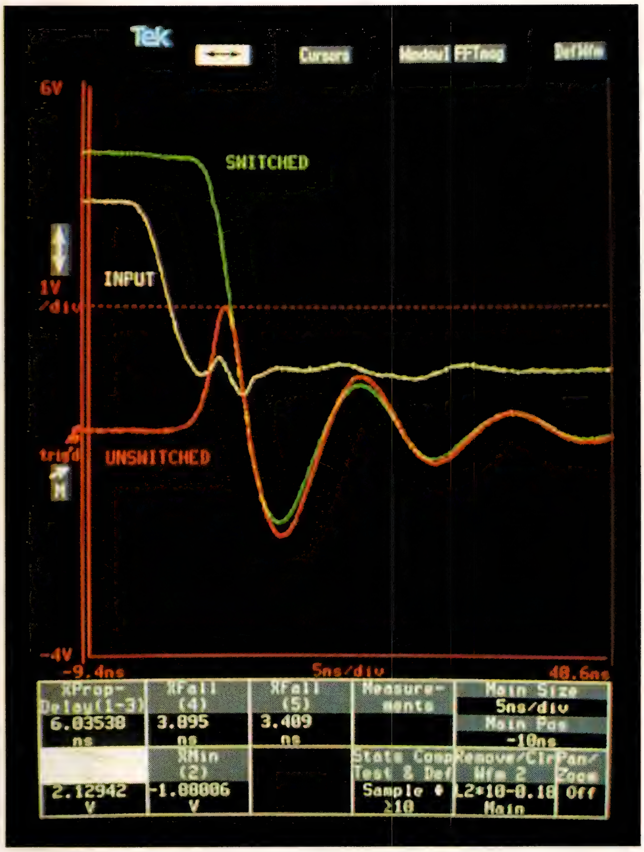
IN
OV
8

Innovate with 8-bit technology in ways you never dreamed possible. You'll get an idea just how, starting May 10.

MOTOROLA

Motorola AC

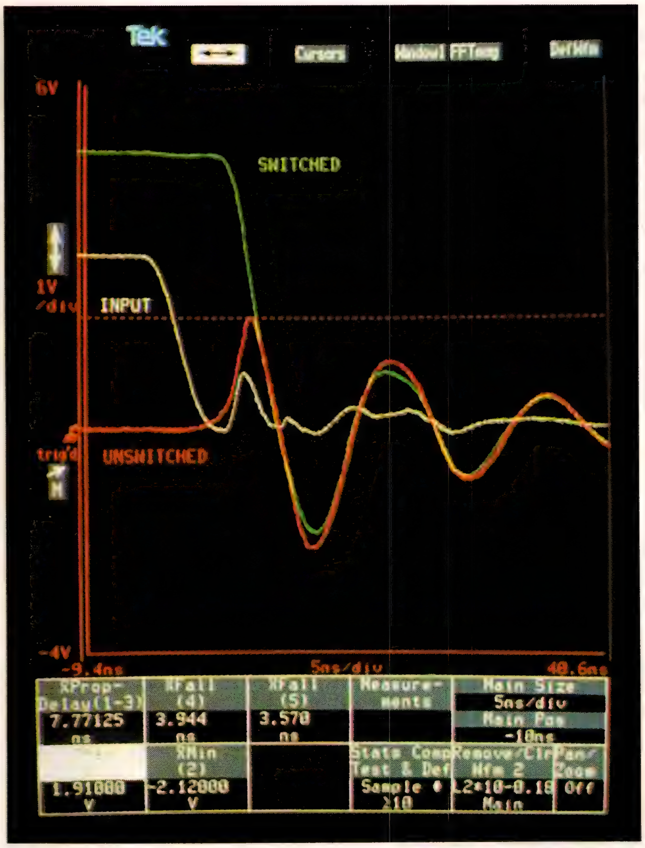
	DEVICE	
	MC74AC244N	**MC74AC244DW**
$V_{OLP\text{-}HL}$ (V)	2.12	1.96
$V_{OLP\text{-}LH}$ (V)	1.02	0.92
$V_{OHV\text{-}HL}$ (V)	4.24	4.26
$V_{OHV\text{-}LH}$ (V)	3.50	3.59
t_{PHL} (nsec)	6.0	5.9
t_{PLH} (nsec)	6.7	6.0
t_r (nsec)	4.4	4.0
t_f (nsec)	3.4	3.3
$V_{OLP\text{-}HL} {}^{*} t_{PHL}$	12.7	11.6
FIXTURE	DIP	SOIC



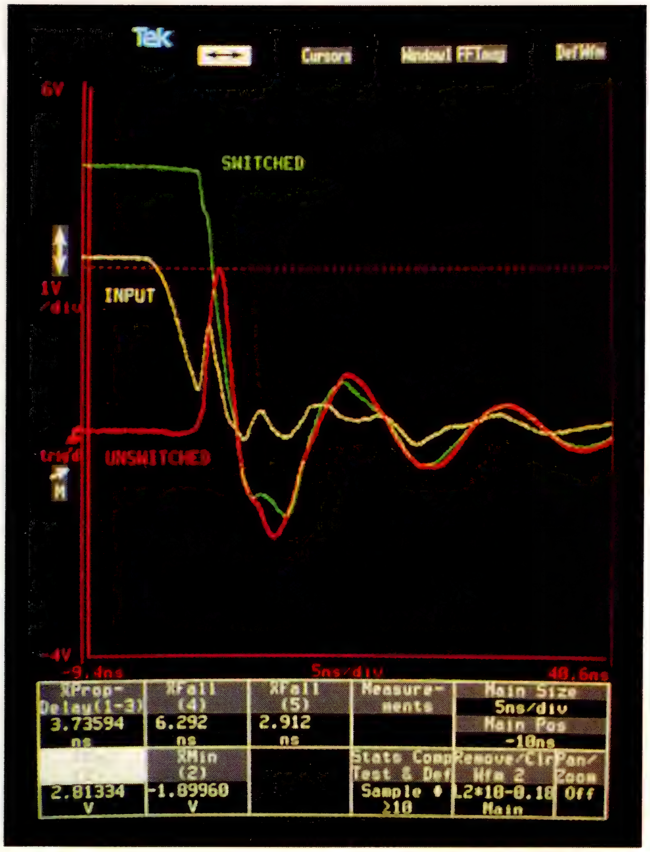
XProp-Delay(1-3) 6.03538 ns
XFall (4) 3.895 ns
XFall (5) 3.409 ns
Measure-ments
Main Size 5ns/div
Main Pos -10ns
2.12942 V
XMin (2) -1.00006 V
State Comp Test & Def Sample ◆ ≥10
Remove/Clr Wfm 2 L2*10-0.18 Main
Pan/Zoom Off

Motorola ACT

	DEVICE	
	MC74ACT244N	**MC74ACT244DW**
$V_{OLP\text{-}HL}$ (V)	1.91	1.58
$V_{OLP\text{-}LH}$ (V)	0.95	0.91
$V_{OHV\text{-}HL}$ (V)	4.18	4.05
$V_{OHV\text{-}LH}$ (V)	3.46	3.52
t_{PHL} (nsec)	7.8	7.6
t_{PLH} (nsec)	6.7	6.0
t_r (nsec)	4.2	3.8
t_f (nsec)	3.6	3.9
$V_{OLP\text{-}HL} {}^{*} t_{PHL}$	14.9	12.0
FIXTURE	DIP	SOIC

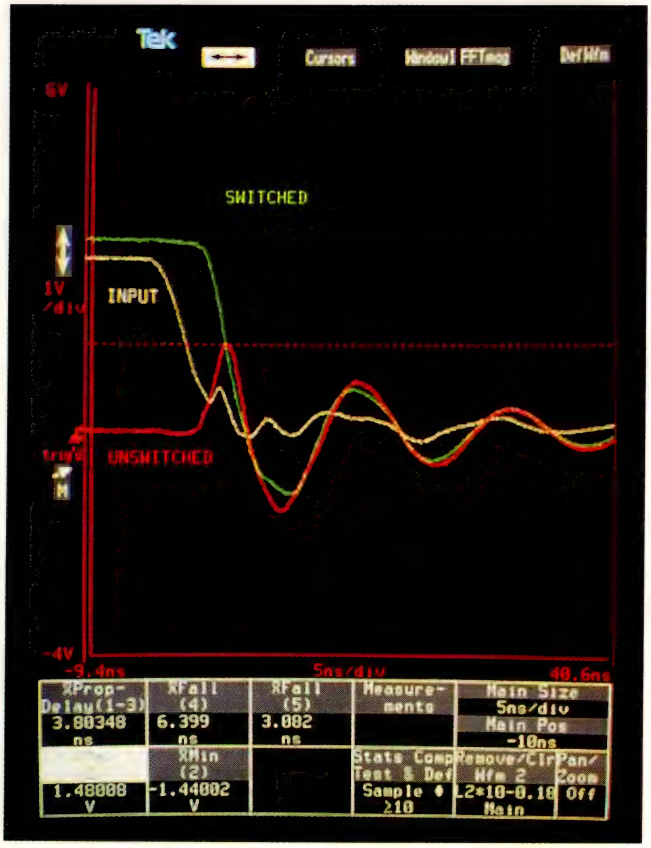


XProp-Delay(1-3) 7.77125 ns
XFall (4) 3.944 ns
XFall (5) 3.570 ns
Measure-ments
Main Size 5ns/div
Main Pos -10ns
1.91000 V
XMin (2) -2.12000 V
State Comp Test & Def Sample ◆ ≥10
Remove/Clr Wfm 2 L2*10-0.18 Main
Pan/Zoom Off



IDT FCT

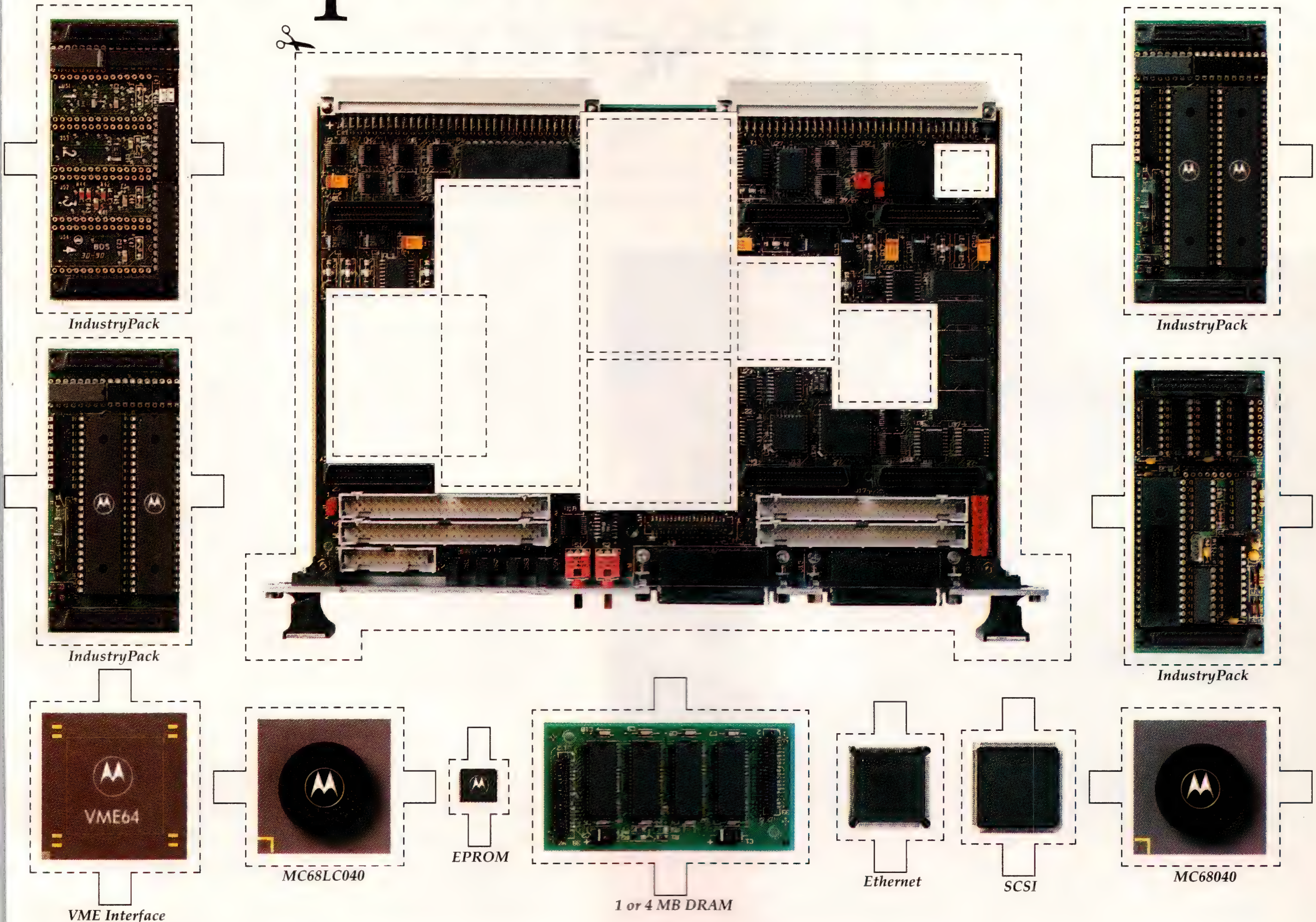
	DEVICE	
	74FCT244P	74FCT244CSO
$V_{OLP\text{-}HL}$ (V)	2.80	2.17
$V_{OLP\text{-}LH}$ (V)	1.09	0.97
$V_{OHV\text{-}HL}$ (V)	1.75	2.92
$V_{OHV\text{-}LH}$ (V)	3.64	3.77
t_{PHL} (nsec)	3.7	3.7
t_{PLH} (nsec)	3.6	3.5
t_r (nsec)	4.5	4.3
t_f (nsec)	2.9	2.9
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	10.4	8.0
FIXTURE	DIP	SOIC



IDT FCTT

	DEVICE		
	74FCT244CTP	74FCT244CTSO	74FCT244CTPY
$V_{OLP\text{-}HL}$ (V)	1.48	1.27	1.42
$V_{OLP\text{-}LH}$ (V)	1.05	0.98	1.11
$V_{OHV\text{-}HL}$ (V)	3.13	3.13	2.99
$V_{OHV\text{-}LH}$ (V)	2.95	3.09	2.97
t_{PHL} (nsec)	3.8	3.7	3.6
t_{PLH} (nsec)	3.9	3.4	3.1
t_r (nsec)	4.2	4.2	4.1
t_f (nsec)	3.1	3.1	3.3
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	5.6	4.7	5.1
FIXTURE	DIP	SOIC	SSOP

So you think you can design a better embedded computer than we can?



Of course you can. And we'll even help you. With the new MVME162 Embedded Computer.

The MVME162 is modular. Adaptable. So that you can select the exact functionality you want, without paying for features you don't need.

Now, would you like your MVME162 with a 68040 CPU (with floating point) or a 68LC040 CPU (no floating point)? VME bus or no bus? One, two, three, or four IndustryPack™ modules? Synchronous or Asynchronous serial ports? Ethernet or SCSI? 1MB DRAM or 4MB? 512K or 2MB of SRAM? And what other functions would you like with that?

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About the only thing that's not optional is Motorola's unmatched single board computer expertise, breakthrough engineering, outstanding performance and unwavering commitment to quality.

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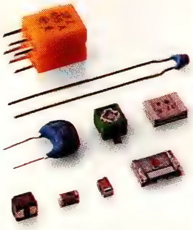
CIRCLE NO. 30

Designing automotive subsystems? Here's how to achieve global presence.

More and more, improving – or even maintaining – your position in the automotive market calls for some deft maneuvering on an around-the-world basis. And that's precisely where Murata Erie can be a valuable ally.

You see, with us as your passive component source, you can count on complete and easily accessed support no matter where your manufacturing and marketing roads lead. Whether you're making trip/navigation computers in Nürnberg, sensors in Seoul or emission controls in Canada.

And, more than worldwide manufacturing resources, we mean technical support as well. So whether you're designing – or redesigning – an engine control system, CD player or cellular telephone, we'll be there. And we'll put nearly a half-century of technological expertise and leadership to work for you, plus all the advantages of Murata Erie's 1.0 QRS (100% quality, reliability, service) program.



A final, important point. Because our component line is a massive one, from chip caps to piezoelectric gyroscope systems, it offers real opportunities to gain measurable economic ground while achieving vendor reduction goals.

Call or write for details: Murata Erie North America, Marketing Communications, 2200 Lake Park Drive, Smyrna, GA 30080; 1-800-831-9172, Fax: 1-404-684-1541. Because, when it comes to global presence, it's best to travel with people who have it.

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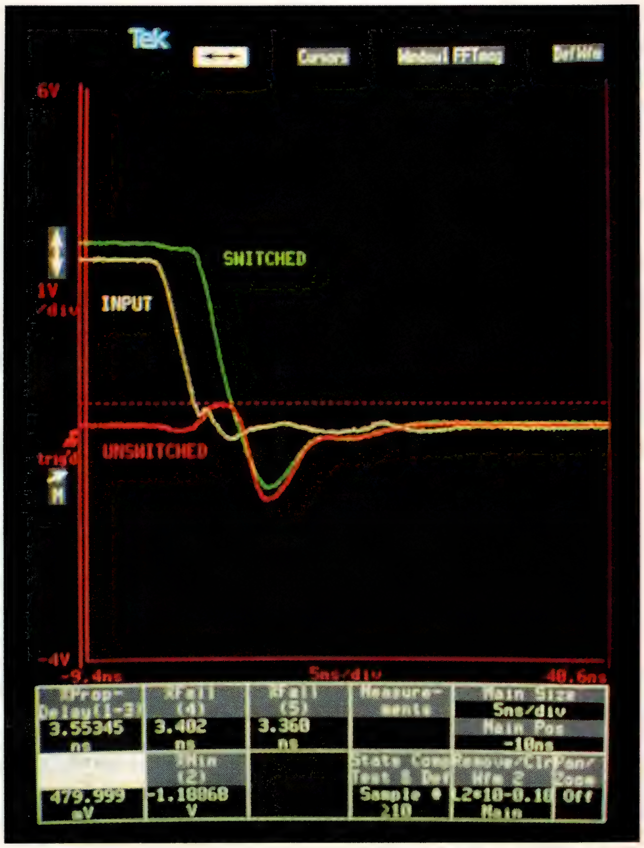
Delivering Technology Worldwide℠

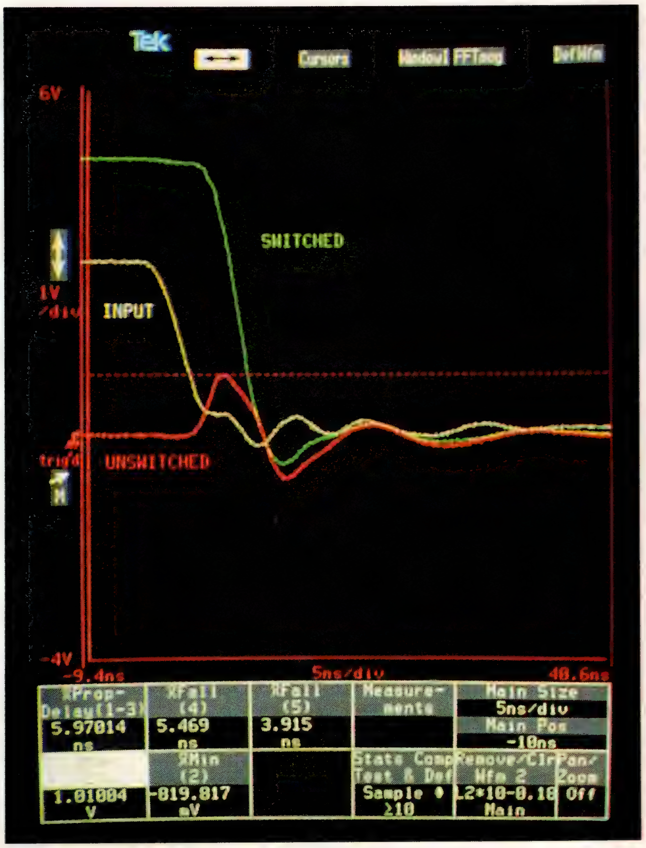
CIRCLE NO. 81



National ABT

	DEVICE	
	74ABT244CSC[1]	74ABT2244CSC
$V_{OLP\text{-}HL}$ (V)	0.47	0.37
$V_{OLP\text{-}LH}$ (V)	0.36	0.36
$V_{OHV\text{-}HL}$ (V)	3.05	3.08
$V_{OHV\text{-}LH}$ (V)	2.95	2.97
t_{PHL} (nsec)	3.6	4.1
t_{PLH} (nsec)	3.8	3.7
t_r (nsec)	3.6	3.6
t_f (nsec)	3.4	4.4
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	1.7	1.5
FIXTURE	SOIC	SOIC

Note: 1. National Semiconductor's ABT family does not come in a DIP.

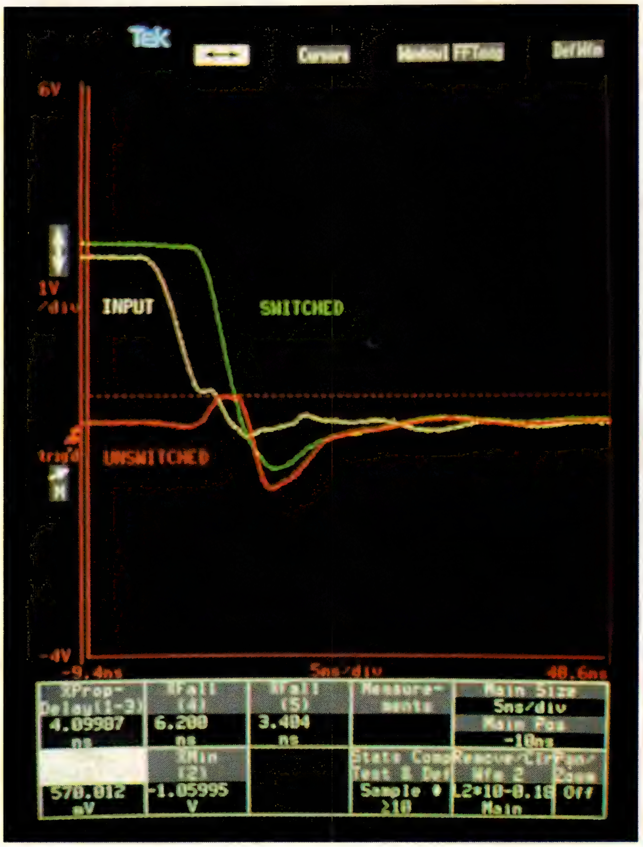


National ACTQ

	DEVICE		
	74ACTQ244PC	74ACTQ244SC	74ACTQ244QSC
$V_{OLP\text{-}HL}$ (V)	1.02	0.90	0.82
$V_{OLP\text{-}LH}$ (V)	0.82	0.86	0.55
$V_{OHV\text{-}HL}$ (V)	4.02	3.99	4.19
$V_{OHV\text{-}LH}$ (V)	3.72	3.71	3.81
t_{PHL} (nsec)	6.0	6.0	6.1
t_{PLH} (nsec)	5.1	4.4	4.5
t_r (nsec)	4.9	4.4	5.0
t_f (nsec)	3.9	4.0	4.6
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	6.1	5.4	5.0
FIXTURE	DIP	SOIC	QSOP

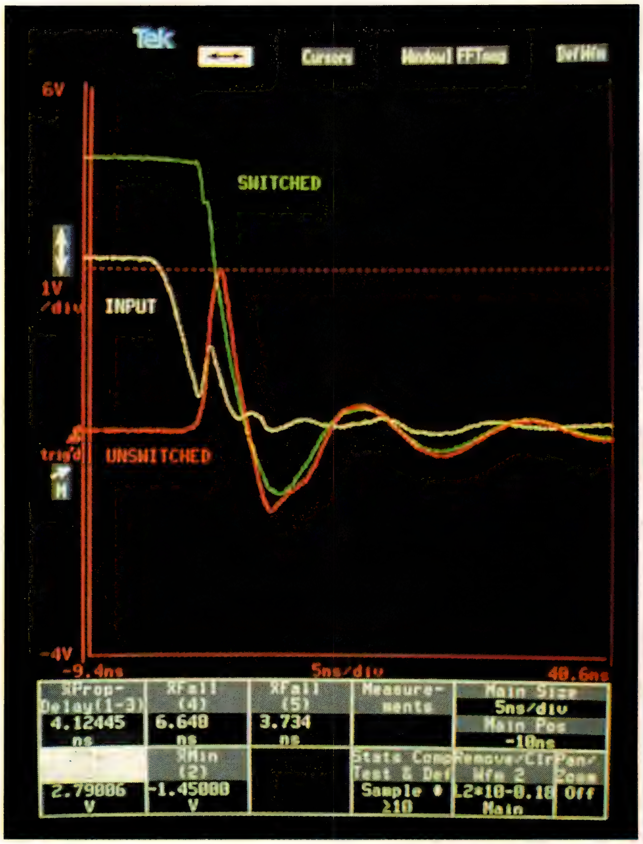
National BCT

	DEVICE			
	74BCT244PC	74BCT244SC	74BCT2244PC	74BCT2244SC
$V_{OLP\text{-}HL}$ (V)	0.58	0.41	0.45	0.33
$V_{OLP\text{-}LH}$ (V)	0.37	0.37	0.35	0.34
$V_{OHV\text{-}HL}$ (V)	2.96	2.87	3.00	2.91
$V_{OHV\text{-}LH}$ (V)	2.73	2.81	2.74	2.83
t_{PHL} (nsec)	4.1	3.9	4.5	4.3
t_{PLH} (nsec)	3.9	3.5	3.8	3.7
t_r (nsec)	4.8	4.5	4.7	4.5
t_f (nsec)	3.4	3.7	4.6	4.5
$V_{OLP\text{-}HL}{}^*t_{PHL}$	2.4	1.6	2.0	1.4
FIXTURE	DIP	SOIC	DIP	SOIC



National FCT

	DEVICE		
	74FCT244PC	74FCT244APC	74FCT244AQSC
$V_{OLP\text{-}HL}$ (V)	1.24	2.80	2.42
$V_{OLP\text{-}LH}$ (V)	0.96	1.17	0.94
$V_{OHV\text{-}HL}$ (V)	4.20	3.88	3.82
$V_{OHV\text{-}LH}$ (V)	3.64	3.52	3.54
t_{PHL} (nsec)	5.3	4.0	3.9
t_{PLH} (nsec)	4.8	4.4	3.7
t_r (nsec)	4.5	4.4	4.5
t_f (nsec)	4.0	3.7	4.0
$V_{OLP\text{-}HL}{}^*t_{PHL}$	6.6	11.2	9.4
FIXTURE	DIP	DIP	QSOP



For PCMCIA, Why Leave the Analog World Outside?

Design your 10Base-T or Token Ring interfaces right into a PCMCIA type I or type II package. New, breakthrough analog module designs from Pulse Engineering mean the end of external cable solutions for network magnetic components in PCMCIA applications.

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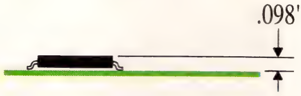
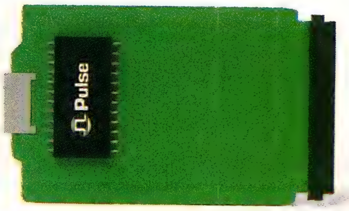
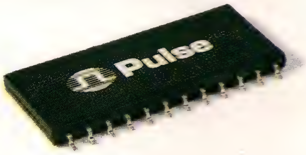
Check out our entire family of PCMCIA network components and modules, presently supporting both 10Base-T and Token Ring over UTP/STP media. For the whole story, call or fax us today.

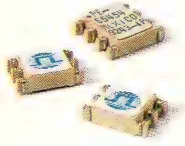




Token Ring
Complete interface magnetics modules contain filters, isolation transformers, common-mode chokes and resistor networks, all designed to match IBM, TI, NSC, and other interface chips. Transmit & receive all in one package only 1.25" x .735" x .098".



Transformers
Tiny surface mount packages under 0.1" high come in a variety of single, dual, and triple configurations. For those who want discrete component solutions for PCMCIA communications applications.



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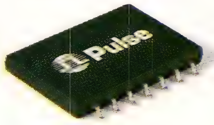
Complete magnetics modules include pre-distortion resistors, low pass filters, isolation transformers and common mode chokes for both transmit and receive channels in a single .800 x .675 x .094" package. Designs optimized for AMD, NSC, AT&T, Level One, or NCR integrated circuits.



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PC Card
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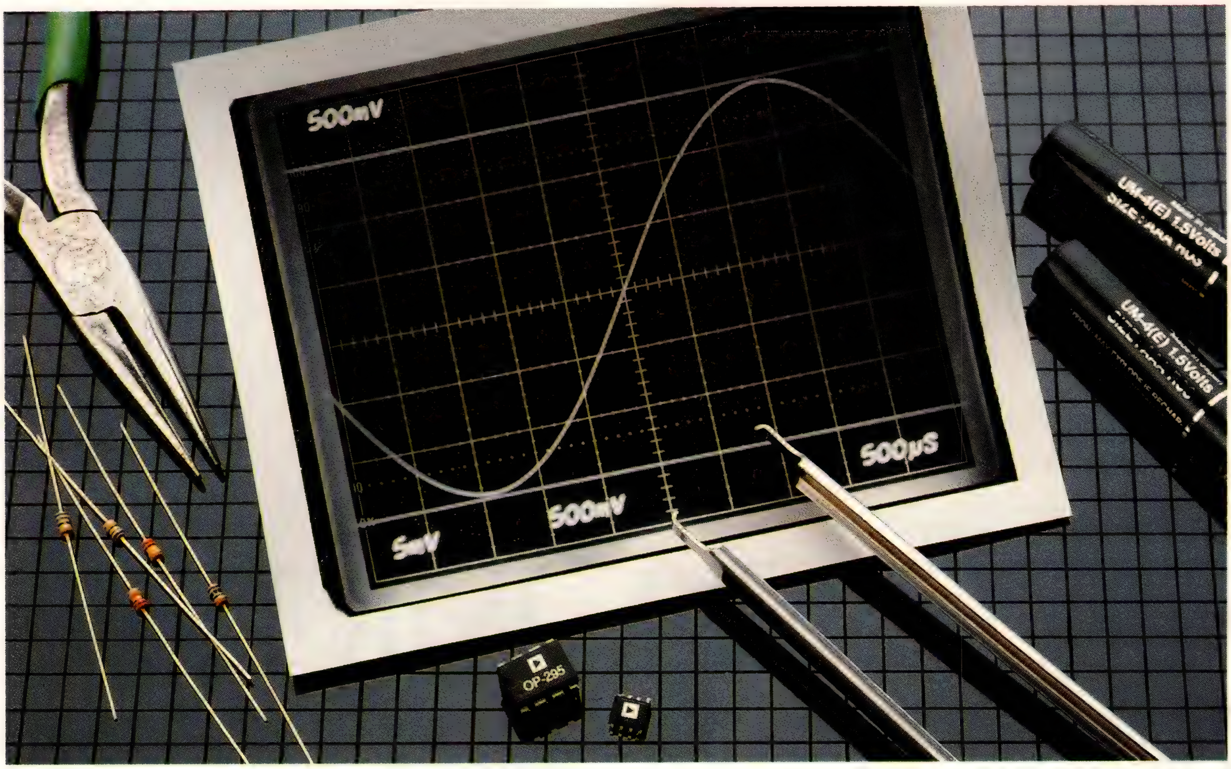
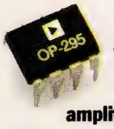
CIRCLE NO. 82

The OP-295 single supply, 3 V op amp.



All the performance of dual supply, with none of the negatives.

Why compromise? With the OP-295 you get dual-supply performance with the simplicity, space and cost savings of a single power supply. Fully specified at +3 V, +5 V and ±15 V, the OP-295 is a dual, rail-to-rail output op amp that combines precision, high output swing and wide dynamic range. And at +3 V, the OP-295 offers unmatched accuracy. Power dissipation at +3 V is 1 mW–ideal for portable applications–and the BiCMOS design yields the industry's lowest offset voltage of 100 µV with only 1.0 µV/°C offset voltage drift.



BiCMOS OP-295

The BiCMOS OP-295 eliminates the negatives common to CMOS rail-to-rail amplifiers; overcoming problems with offset drift, stability while driving capacitive loads, limited supply range and low gain. The OP-295's output swing is larger too, and yet it consumes less than 1/3 the power of competitive CMOS amplifiers.

The OP-295 is the latest in a family of single supply, +3 V products from Analog Devices: other members include single, dual and quad op amps, instrumentation amps, voltage references, switches, converters and DSPs.

The OP-295 is available now in 8-pin DIP and SO packages at $1.98 (in 1,000s). And a quad version is coming soon in 14-pin DIP and 16-pin SO packages. For data sheets, samples and more information call 800-ANALOG-D, or your local distributor listed below.

ANALOG DEVICES

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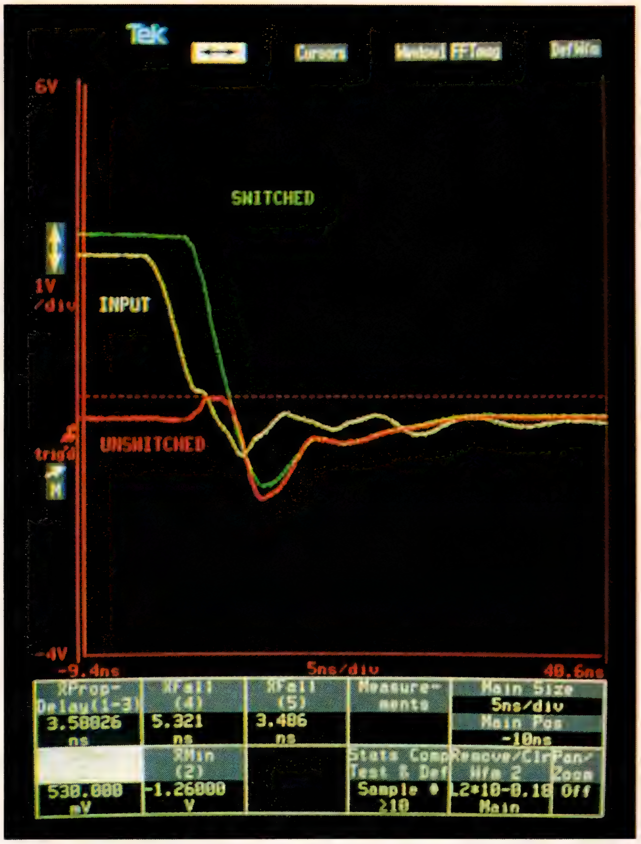
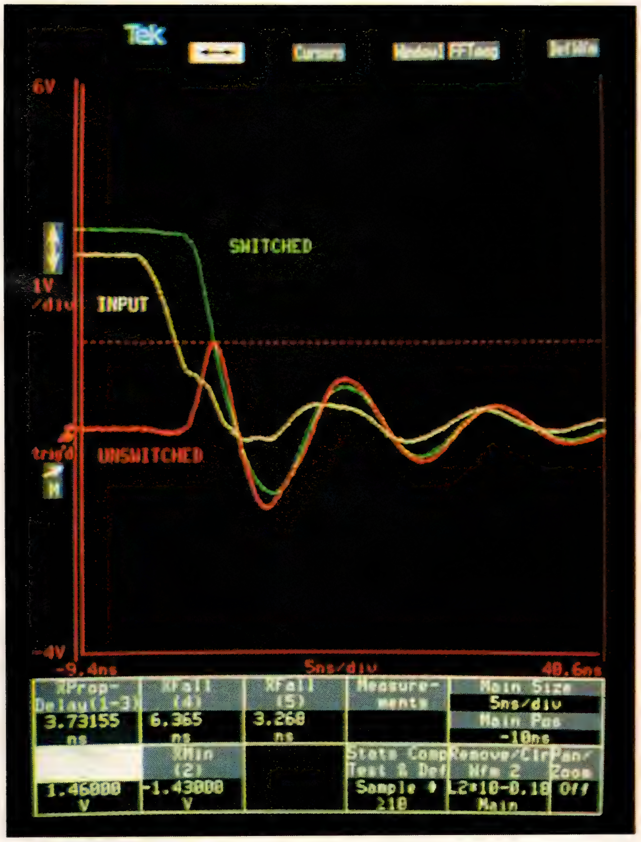
CIRCLE NO. 83



XProp-Delay(1-3) 3.58026 ns
XFall (4) 5.321 ns
XFall (5) 3.486 ns
530.000 mV
XMin (2) -1.26000 V
Main Size 5ns/div
Main Pos -10ns
Sample # 210
L2*10-0.18 Main

Philips ABT

	DEVICE		
	74ABT244N	74ABT244D	74ABT244D-SSOP
$V_{OLP\text{-}HL}$ (V)	0.52	0.35	0.41
$V_{OLP\text{-}LH}$ (V)	0.38	0.26	0.35
$V_{OHV\text{-}HL}$ (V)	3.21	3.08	3.12
$V_{OHV\text{-}LH}$ (V)	2.97	2.98	2.97
t_{PHL} (nsec)	3.6	4.1	4.1
t_{PLH} (nsec)	3.1	3.9	3.1
t_r (nsec)	4.0	3.8	3.7
t_f (nsec)	3.5	3.8	3.6
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	1.9	1.4	1.7
FIXTURE	DIP	SOIC	SSOP



XProp-Delay(1-3) 3.73155 ns
XFall (4) 6.365 ns
XFall (5) 3.268 ns
1.46000 V
XMin (2) -1.43000 V
Main Size 5ns/div
Main Pos -10ns
Sample # 210
L2*10-0.18 Main

Pioneer FCTT

	DEVICE		
	PI74FCT244TP	PI74FCT244DTP	PI74FCT244TS
$V_{OLP\text{-}HL}$ (V)	1.27	1.47	1.22
$V_{OLP\text{-}LH}$ (V)	0.80	0.85	0.74
$V_{OHV\text{-}HL}$ (V)	3.18	3.25	3.07
$V_{OHV\text{-}LH}$ (V)	2.95	3.03	2.97
t_{PHL} (nsec)	4.2	3.7	4.0
t_{PLH} (nsec)	4.1	3.7	3.6
t_r (nsec)	3.6	3.6	3.4
t_f (nsec)	3.6	3.3	3.8
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	5.3	5.4	4.9
FIXTURE	DIP	DIP	SOIC

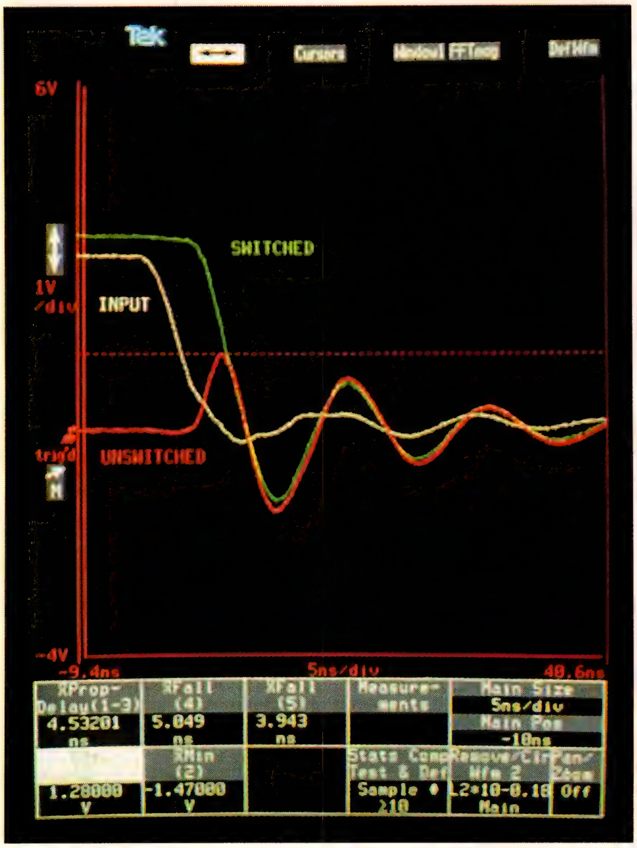
Pioneer FCTT

	DEVICE		
	PI74FCT244DTS	PI74FCT244TQ	PI74FCT244DTQ
$V_{OLP\text{-}HL}$ (V)	1.38	1.23	1.14
$V_{OLP\text{-}LH}$ (V)	0.75	0.63	0.52
$V_{OHV\text{-}HL}$ (V)	3.15	3.25	3.05
$V_{OHV\text{-}LH}$ (V)	3.05	3.10	2.90
t_{PHL} (nsec)	3.7	4.0	4.1
t_{PLH} (nsec)	3.4	3.1	3.7
t_r (nsec)	3.4	3.6	3.5
t_f (nsec)	3.7	3.9	3.8
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	5.1	4.9	4.7
FIXTURE	SOIC	QSOP	QSOP

Quality FCTT

	DEVICE		
	QS74FCT244CTP	QS74FCT244DTSO	QS74FCT244CTQ[1]
$V_{OLP\text{-}HL}$ (V)	1.28	1.37	1.73
$V_{OLP\text{-}LH}$ (V)	0.50	0.38	0.51
$V_{OHV\text{-}HL}$ (V)	3.11	3.07	3.43
$V_{OHV\text{-}LH}$ (V)	2.88	2.96	3.28
t_{PHL} (nsec)	4.5	4.4	4.1
t_{PLH} (nsec)	4.8	4.1	2.8
t_r (nsec)	4.1	3.9	3.7
t_f (nsec)	3.9	3.8	3.7
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	5.8	6.0	7.1
FIXTURE	DIP	SOIC	QSOP

Note: [1]See text concerning results.



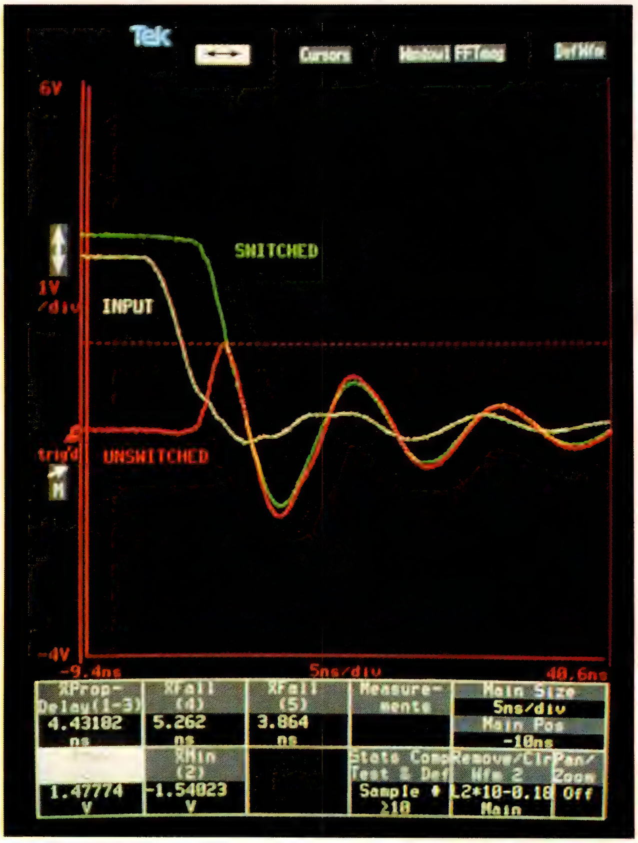
XProp-Delay(1-3) 4.53201 ns
XFall (4) 5.049 ns
XFall (5) 3.943 ns
Measure-ments
Main Size 5ns/div
Main Pos -10ns
1.28000 V
XMin (2) -1.47000 V
Stats Comp Test & Def Sample # ≥10
Remove/Clr Wfm 2 L2*10-0.10 Main
Pan/Zoom Off

Quality FCTT

	DEVICE		
	QS74FCT2244CTP	QS74FCT2244CTSO	QS74FCT2244CTQ
$V_{OLP\text{-}HL}$ (V)	0.80	0.64	0.73
$V_{OLP\text{-}LH}$ (V)	0.62	0.31	0.43
$V_{OHV\text{-}HL}$ (V)	3.28	3.07	3.24
$V_{OHV\text{-}LH}$ (V)	3.00	2.93	3.07
t_{PHL} (nsec)	4.6	4.9	4.6
t_{PLH} (nsec)	4.4	4.2	3.8
t_r (nsec)	3.5	3.8	3.5
t_f (nsec)	3.9	4.5	4.2
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	3.7	3.1	3.4
FIXTURE	DIP	SOIC	QSOP

Seiko FCT

	DEVICE		
	S74FCT244A	S74FCT244CJF	S74FCT244ATS
$V_{OLP\text{-}HL}$ (V)	1.49	1.40	1.31
$V_{OLP\text{-}LH}$ (V)	0.51	0.44	0.37
$V_{OHV\text{-}HL}$ (V)	3.13	3.10	3.18
$V_{OHV\text{-}LH}$ (V)	2.88	2.98	3.01
t_{PHL} (nsec)	4.4	4.4	4.4
t_{PLH} (nsec)	4.7	4.0	3.9
t_r (nsec)	4.1	3.8	4.1
t_f (nsec)	3.9	3.9	4.0
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	6.6	6.2	5.8
FIXTURE	DIP	SOIC	QSOP



XProp-Delay(1-3) 4.43182 ns
XFall (4) 5.262 ns
XFall (5) 3.864 ns
Measure-ments
Main Size 5ns/div
Main Pos -10ns
1.47774 V
XMin (2) -1.54023 V
Stats Comp Test & Def Sample # ≥10
Remove/Clr Wfm 2 L2*10-0.10 Main
Pan/Zoom Off

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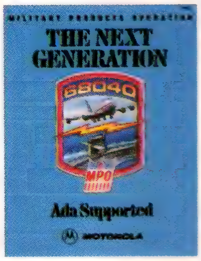
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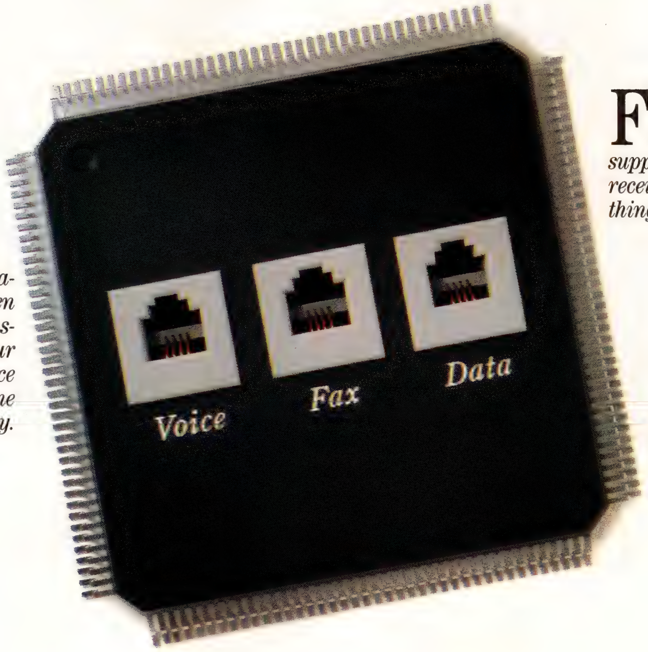

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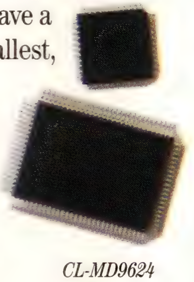

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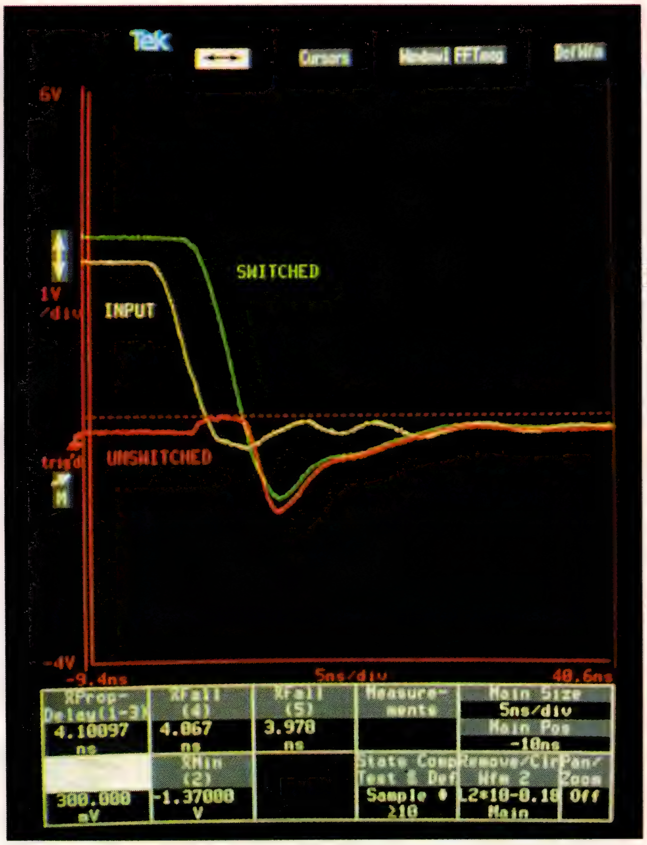
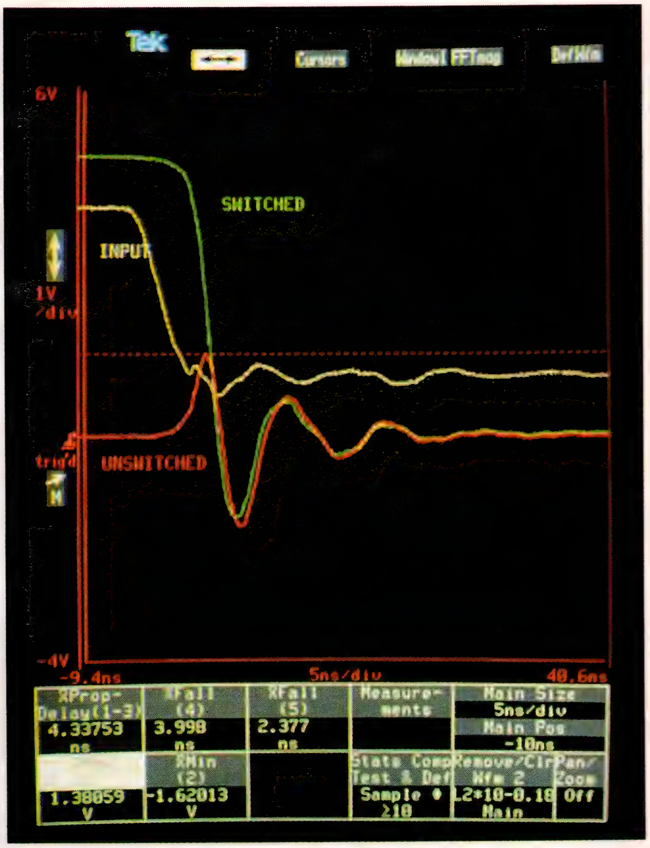


XProp-Delay(1-3) 4.10097 ns
XFall (4) 4.067 ns
XFall (5) 3.978 ns
300.000 mV
XMin (2) -1.37000 V
Measure-ments
Main Size 5ns/div
Main Pos -10ns
State Comp Test & Def Sample ♦ ≥10
Remove/Clr Wfm 2 L2*10-0.1♦ Main
Pan/Zoom Off

TI ABT

	DEVICE		
	SN74ABT244N	SN74ABT244DW	SN74ABT244DBLE
$V_{OLP\text{-}HL}$ (V)	0.30	0.30	0.31
$V_{OLP\text{-}LH}$ (V)	0.27	0.28	0.34
$V_{OHV\text{-}HL}$ (V)	3.29	3.21	3.19
$V_{OHV\text{-}LH}$ (V)	3.14	3.14	3.09
t_{PHL} (nsec)	4.1	4.1	4.2
t_{PLH} (nsec)	4.2	3.9	3.8
t_r (nsec)	3.8	4.7	4.6
t_f (nsec)	4.0	4.0	4.0
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	1.2	1.2	1.3
FIXTURE	DIP	SOIC	SSOP



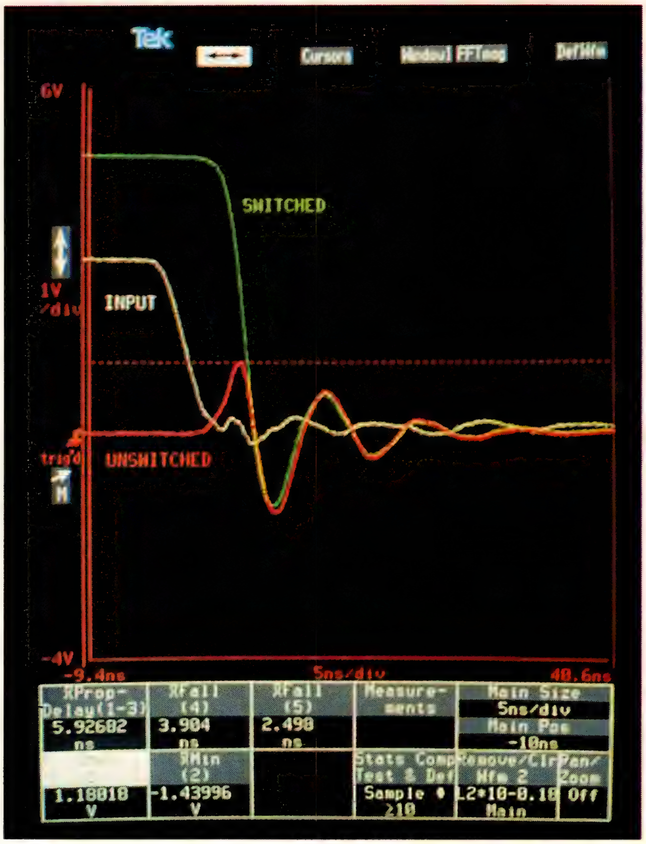
XProp-Delay(1-3) 4.33753 ns
XFall (4) 3.998 ns
XFall (5) 2.377 ns
1.38059 V
XMin (2) -1.62013 V
Measure-ments
Main Size 5ns/div
Main Pos -10ns
State Comp Test & Def Sample ♦ ≥10
Remove/Clr Wfm 2 L2*10-0.1♦ Main
Pan/Zoom Off

TI AC

	DEVICE			
	74AC11244NT	74AC11244DW	74AC11244DBLE	74AC11244PWLE
$V_{OLP\text{-}HL}$ (V)	1.38	0.90	0.95	0.74
$V_{OLP\text{-}LH}$ (V)	0.31	0.18	0.18	0.16
$V_{OHV\text{-}HL}$ (V)	4.07	4.20	4.18	4.21
$V_{OHV\text{-}LH}$ (V)	3.36	3.85	3.69	3.85
t_{PHL} (nsec)	4.3	4.6	4.3	4.2
t_{PLH} (nsec)	4.9	5.4	5.0	5.1
t_r (nsec)	3.3	4.0	3.9	3.9
t_f (nsec)	2.4	3.0	2.7	2.8
$V_{OLP\text{-}HL}{}^{*}t_{PHL}$	5.9	4.1	4.1	3.1
FIXTURE	DIP	SOIC	SSOP	TSSOP

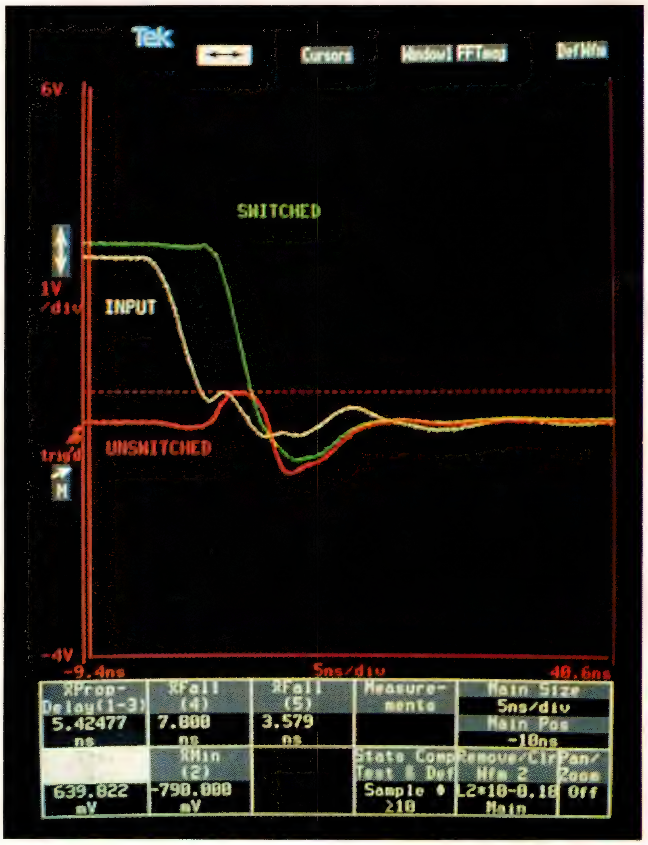
TI ACT

	DEVICE			
	74ACT11244N	74ACT11244DW	74ACT11244DBLE	74ACT11244PWLE
$V_{OLP\text{-}HL}$ (V)	1.20	1.06	0.90	0.66
$V_{OLP\text{-}LH}$ (V)	0.20	0.13	0.11	0.08
$V_{OHV\text{-}HL}$ (V)	4.27	4.17	4.09	4.28
$V_{OHV\text{-}LH}$ (V)	3.50	3.60	3.66	3.88
t_{PHL} (nsec)	5.9	5.6	6.0	6.8
t_{PLH} (nsec)	5.9	5.4	5.7	6.2
t_r (nsec)	3.5	3.7	4.0	4.2
t_f (nsec)	2.5	2.8	2.6	3.0
$V_{OLP\text{-}HL}{}^*t_{PHL}$	7.1	5.9	5.4	4.5
FIXTURE	DIP	SOIC	SSOP	TSSOP



TI BCT

	DEVICE		
	SN74BCT244N	SN74BCT244DW	SN74BCT244DBLE
$V_{OLP\text{-}HL}$ (V)	0.65	0.52	0.48
$V_{OLP\text{-}LH}$ (V)	0.44	0.41	0.44
$V_{OHV\text{-}HL}$ (V)	2.81	2.80	2.76
$V_{OHV\text{-}LH}$ (V)	2.88	2.94	2.92
t_{PHL} (nsec)	5.4	4.9	5.0
t_{PLH} (nsec)	3.9	3.6	3.4
t_r (nsec)	4.6	4.7	4.2
t_f (nsec)	3.6	3.9	4.0
$V_{OLP\text{-}HL}{}^*t_{PHL}$	3.5	2.5	2.4
FIXTURE	DIP	SOIC	SSOP



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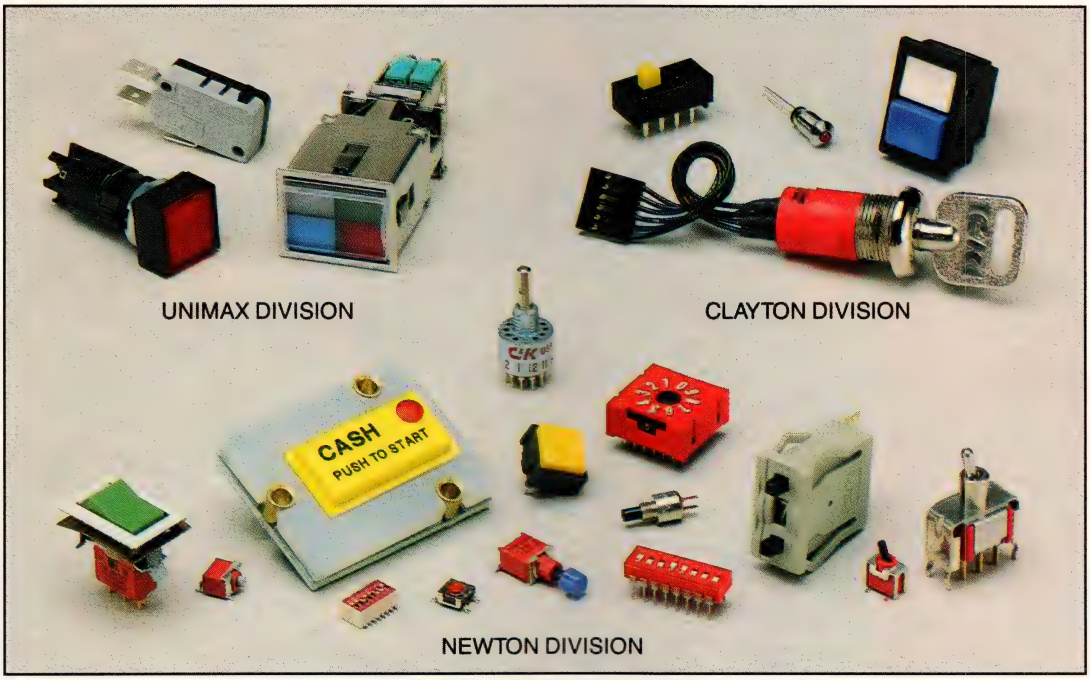

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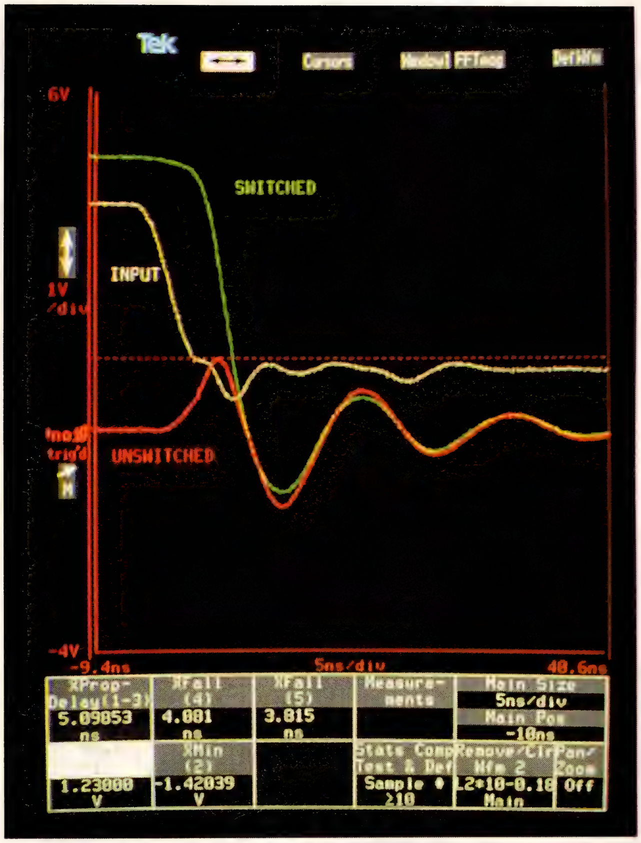
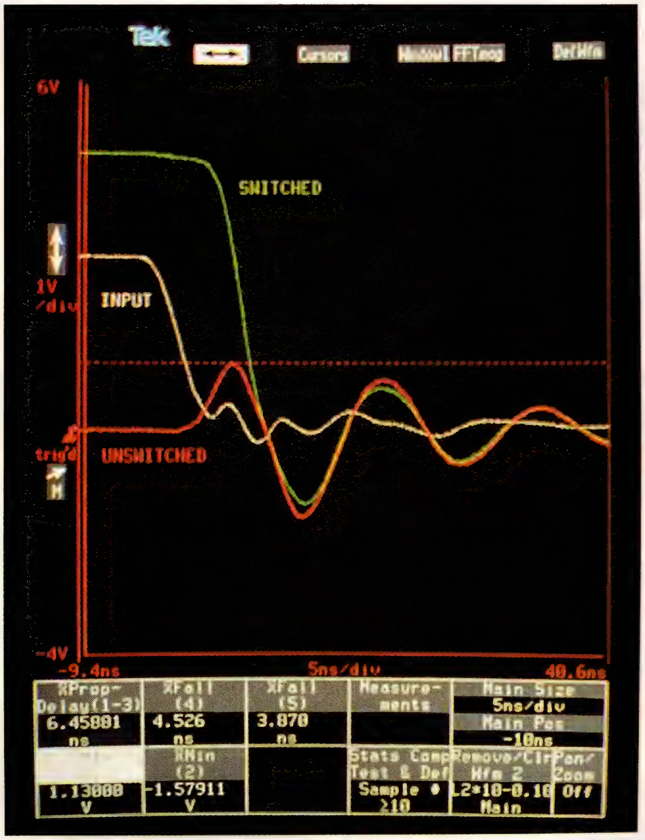


```
%Prop-      %Fall    %Fall   Measure-        Main Size
Delay(1-3)  (4)      (5)     ments           5ns/div
5.09853     4.001    3.815                   Main Pos
ns          ns       ns                      -10ns
            %Min             Stats Comp Remove/Clr Pan/
            (2)              Test & Def Wfm 2      Zoom
1.23000     -1.42039         Sample ●   L2*10-0.10 Off
V           V                ≥10        Main
```

Toshiba AC

	DEVICE		
	TC74AC244P	TC74AC244FW	TC74AC244FS
$V_{OLP\text{-}HL}$ (V)	1.20	0.95	0.85
$V_{OLP\text{-}LH}$ (V)	0.55	0.40	0.45
$V_{OHV\text{-}HL}$ (V)	4.21	4.16	4.16
$V_{OHV\text{-}LH}$ (V)	3.60	3.84	3.80
t_{PHL} (nsec)	5.1	5.9	5.0
t_{PLH} (nsec)	5.9	6.0	5.3
t_r (nsec)	4.6	4.5	4.2
t_f (nsec)	3.8	3.9	3.6
$V_{OLP\text{-}HL}{}^*t_{PHL}$	6.1	5.6	4.3
FIXTURE	DIP	SOIC	TSSOP



```
%Prop-      %Fall    %Fall   Measure-        Main Size
Delay(1-3)  (4)      (5)     ments           5ns/div
6.45881     4.526    3.870                   Main Pos
ns          ns       ns                      -10ns
            %Min             Stats Comp Remove/Clr Pan/
            (2)              Test & Def Wfm 2      Zoom
1.13000     -1.57911         Sample ●   L2*10-0.10 Off
V           V                ≥10        Main
```

Toshiba ACT

	DEVICE	
	TC74ACT244P	TC74ACT244FS
$V_{OLP\text{-}HL}$ (V)	1.13	0.87
$V_{OLP\text{-}LH}$ (V)	0.53	0.46
$V_{OHV\text{-}HL}$ (V)	4.19	4.17
$V_{OHV\text{-}LH}$ (V)	3.67	3.73
t_{PHL} (nsec)	6.5	6.1
t_{PLH} (nsec)	5.7	4.4
t_r (nsec)	4.7	4.0
t_f (nsec)	3.9	3.7
$V_{OLP\text{-}HL}{}^*t_{PHL}$	7.3	5.3
FIXTURE	DIP	TSSOP

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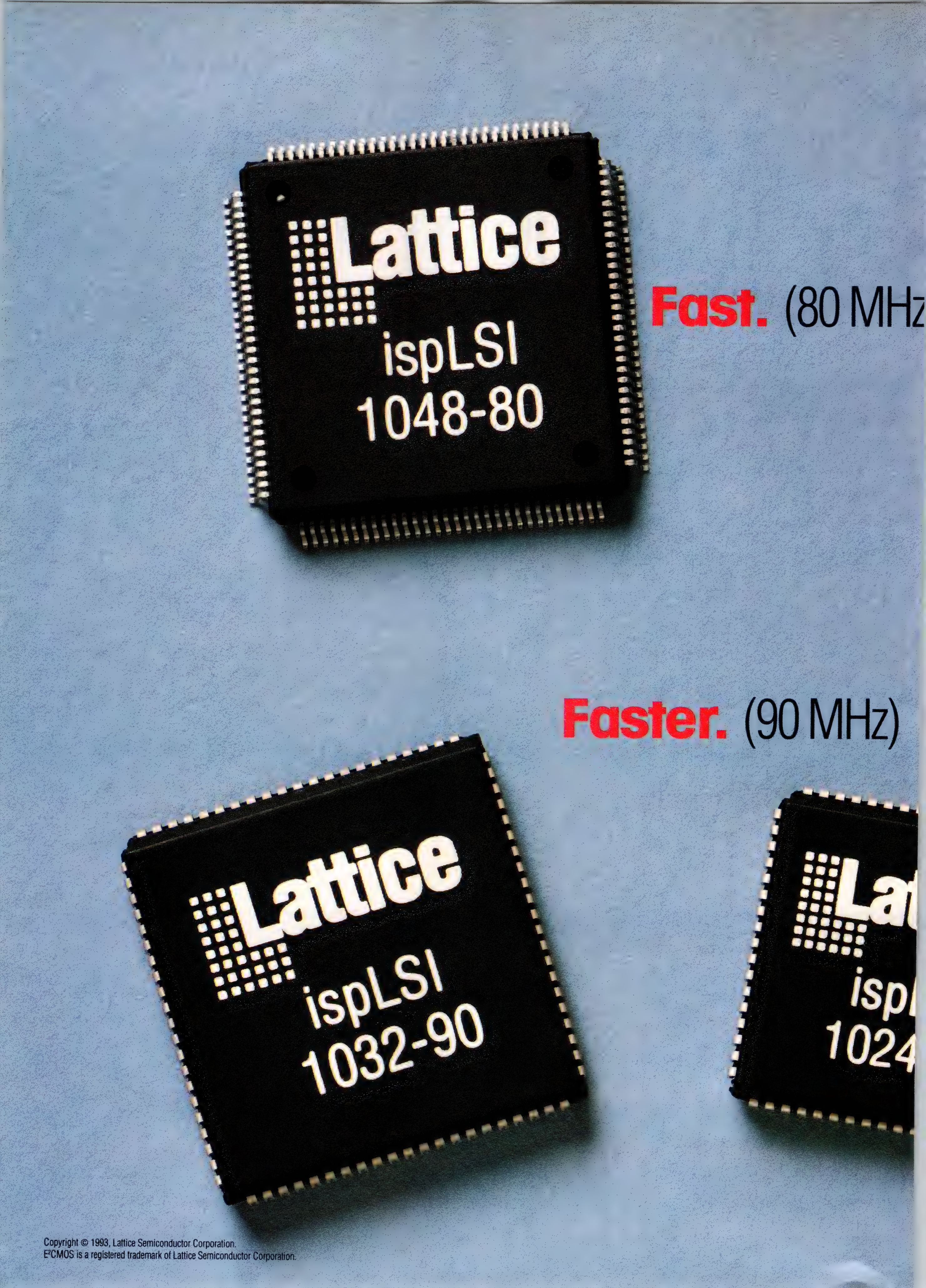

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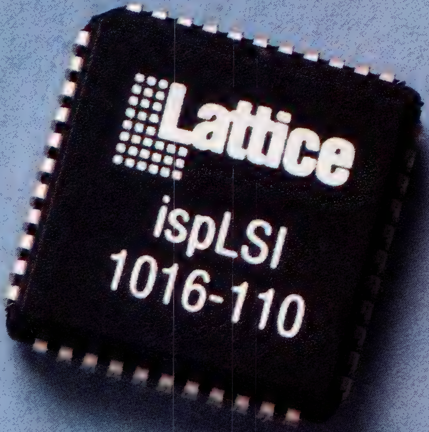

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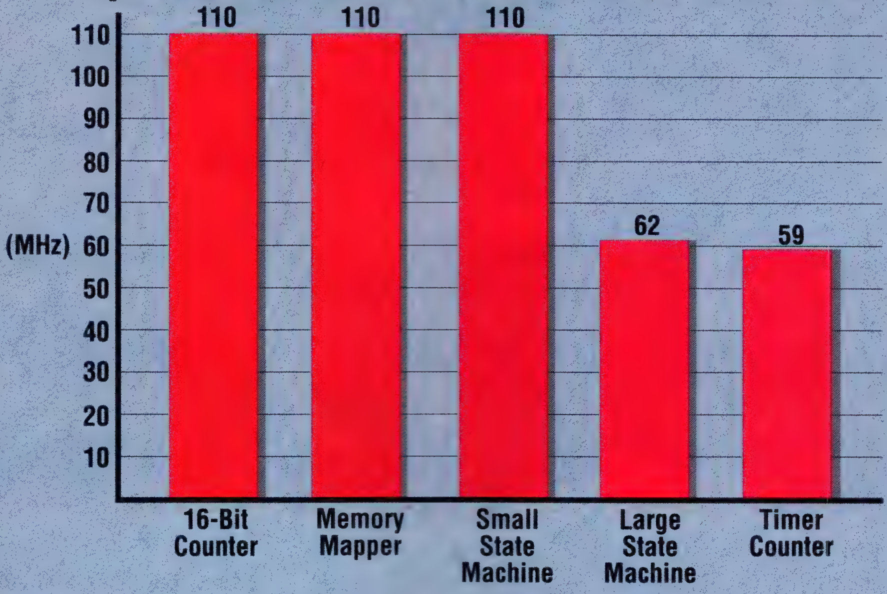

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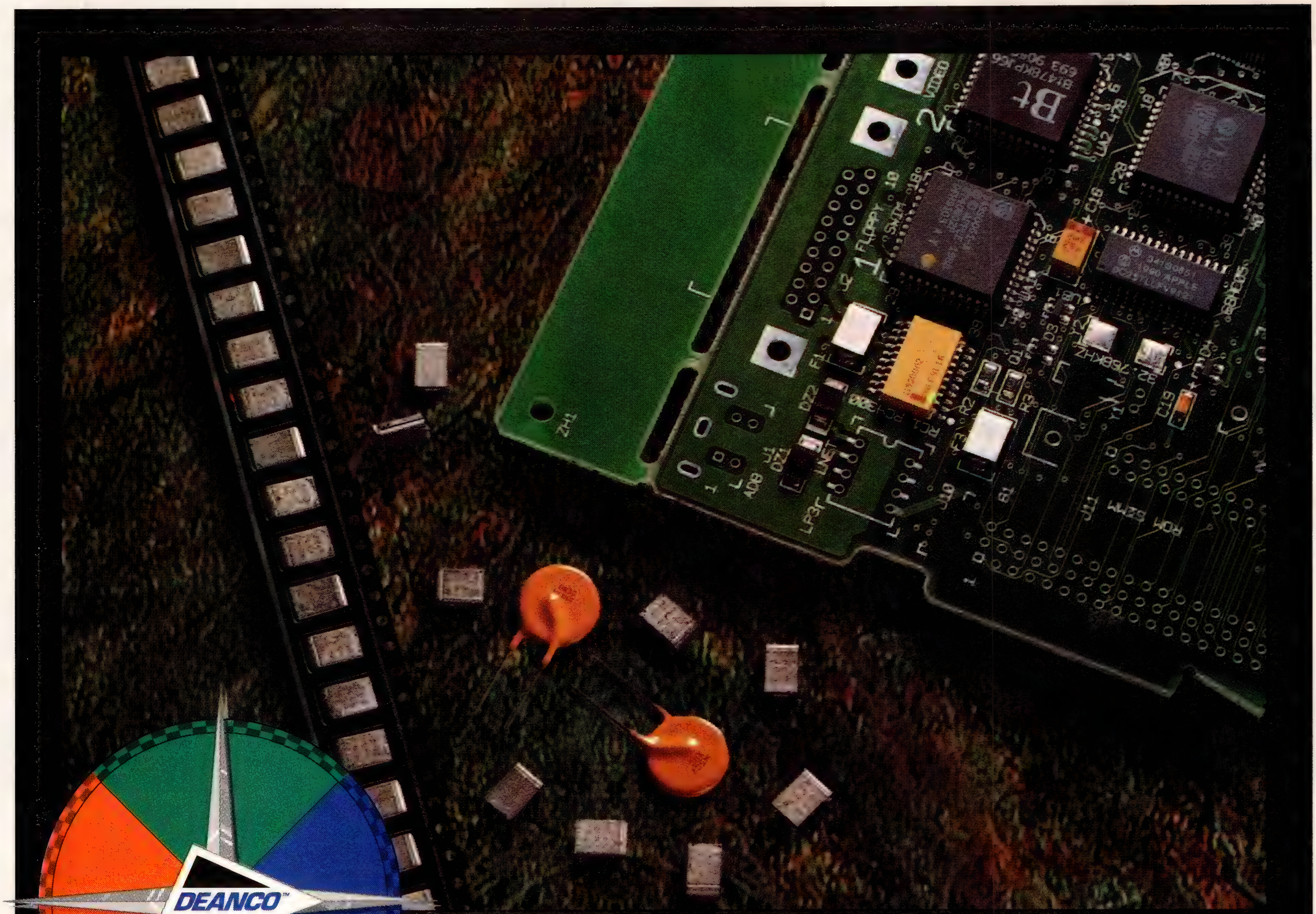

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Electro/93

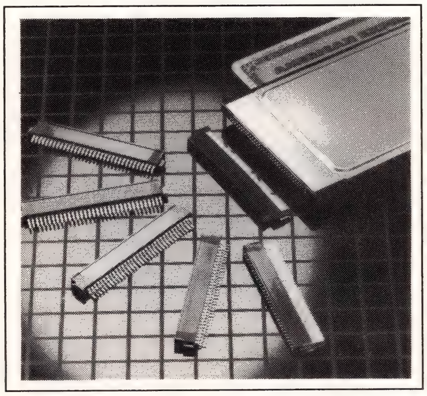
THE SHOW, THE PRODUCTS

Virtual reality, artificial neural networks, DSP tools, HDTV—these are only a few of the leading-edge technology topics on tap for the Electro/93 conference. The show, scheduled for April 27 to 29, at the Raritan Center in Edison, NJ, combines more than 500 exhibiting companies and 29 technical sessions to form the Northeast's largest electronics conference and exhibition.

The technical-session program will extend over the three days of the show. In the computer-technology track, you will hear discussions on 64-bit processing; understanding high-density programmable logic; new FPGA architectures; and new PC technology. The communications track will cover lightwave communications; commercial applications of microwave technology; and video distribution over ordinary wire. The advanced-technologies track will get into virtual reality; high-performance batteries; HDTV; and medical imaging. A track on competitiveness topics and one on general-interest engineering subjects round out the technical-session part of the show.

Giving attendees a glimpse at new products is the other part of the exhibition. Keep reading for a preview of some of the products that are slated to be exhibited at Electro/93.

For more information on any aspect of this year's conference, call (800) 877-2668, or send a fax to (310) 641-5117. EDN



Memory-card socket connector

Series 950 68-position memory-card receptacles feature variable contact tail configurations that offer a low-cost alternative for custom applications. The mold design provides variable-mounting styles; the independent dual-beam contact design ensures redundant electrical contacts and good mechanical performance.

The high-density 0.05×0.05-in. contact pitch in the receptacle and mating headers conforms to the PCMCIA, JEIDA, and JEDEC standards. Beryllium copper contacts are rated for 0.5A and are available with a choice of select gold or palladium nickel platings. Operating range spans −55 to +85°C. $1.90 (OEM qty).

Methode Electronics Inc, 7447 W Wilson Ave, Chicago, IL 60656. Phone (708) 867-9600. FAX (708) 867-0435. Booth No. 1201.

Circle No. 400

DC/DC converters

NT Series converters provide 25 to 30W of output power in a 2.02×1.62×0.55-in. package. Each of the single-output models in the line—48S5.5000NT, 48S12.2500NT, 48S15.2000NT—has transient overvoltage-suppressor diode protection at the output terminals. Overcurrent and overtemperature protection circuits are standard in these converters.

The units in the NT line accept 36 to 72V inputs and output 5V at 5A, 12V at 2.5A, or 15V at 2A. Efficiency figures range to 86%, and I/O isolation equals 1544V dc per UL1459. The units operate over a −40 to +90°C range and feature a 6-sided shielded copper case. $63.45. (OEM qty).

Calex Mfg Co Inc, 2401 Stanwell Dr, Concord, CA 94520. Phone (510) 687-4411. FAX (510) 687-3333. Booth No. 2324. **Circle No. 401**

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B+K Precision, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448. FAX (312) 804-9425. Booth No. 1934. **Circle No. 402**

Oscilloscopes

Models 4162 and 4164 oscilloscopes feature 50k words of memory per channel. The 4164 is a full 4-channel instrument; on the 4162, two of the channels have been optimized for electronic-control signal acquisition.

Both units have a variable zoom feature that provides a 1000:1 trace expansion. Both feature a 7-in. screen with an electronically generated graticule. An optional built-in thermal printer or 4-color plotter can produce hard copy. IEEE-488.2 and RS-423 interfaces are provided. Model 4162, $5990; Model 4164, $6990.

Gould Inc, 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. FAX (216) 328-7400. Booth No. 2218. **Circle No. 403**

Keyswitches

ML keyswitches are designed to meet the requirements of notebook computers. The units feature a 3-mm mechanical travel and tactile feel. The gold crosspoint contacts have a 10-million-cycle lifetime rating.

ML Series devices suit pc-board mounting and require no special tooling. The single-pole, normally open switches are rated for 12V ac/dc and 10 mA. Contact force measures 0.353 to 1.2324 oz. The switches do not lose their integrity over time due to exposure to hot and cold temperatures. $0.31 (100,000).

Cherry Electrical Products, 3600 Sunset Ave, Waukegan, IL 60087. Phone (708) 360-3599. FAX (708) 360-3566. Booth No. 2247.

Circle No. 404

DC/DC converters

The fully filtered units in the XW Series of 50 to 60W converters produce output noise levels of 15- to 50-mV p-p. The nine models in the line operate at 85% efficiency and have an isolation-voltage rating that meets UL1459 requirements.

The converters have remote output-voltage sense, output-voltage trim, and an on-off function. Current-limit and self-resetting thermal-overload circuits provide short-circuit protection for the units. Output and input are overvoltage protected with 1500W transient suppressor diodes. $132.30 (100).

Calex Mfg Co Inc, 2401 Stanwell Dr, Concord, CA 94520. Phone (510) 687-4411. FAX (510) 687-3333. Booth No. 2324. **Circle No. 405**

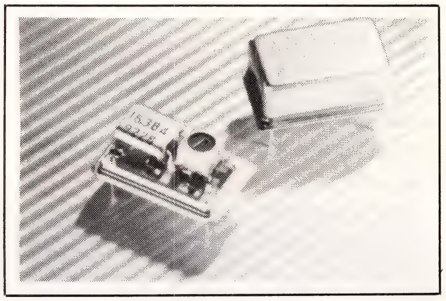
Positioning tables

Series PBC single-axis positioning tables have a lead-screw accuracy of 0.003 in./ft, and linear speeds as high as 50 ft/min. You can easily combine two units to produce an X-Y positioner.

Motor mounting brackets accept NEMA 23 frame-size motors. Load capacities and travel lengths range from 30 to 70 pounds and 2 to 6 in., respectively. You can order tables with lead screws that can advance 0.1 in., 0.2 in., 1 in., 2 mm, and 5 mm per turn. Carriage and base assemblies are fabricated in black anodized aluminum. All rolling elements are hardened stainless steel. $380 for a table with a 4-in. travel, a 50-lb load capacity, and a motor with coupling.

Precision Industrial Components, Box 1004, Middlebury, CT 06762. Phone (203) 758-8272. TWX 710-477-5234. Booth No. 2322.

Circle No. 406



Crystal oscillators

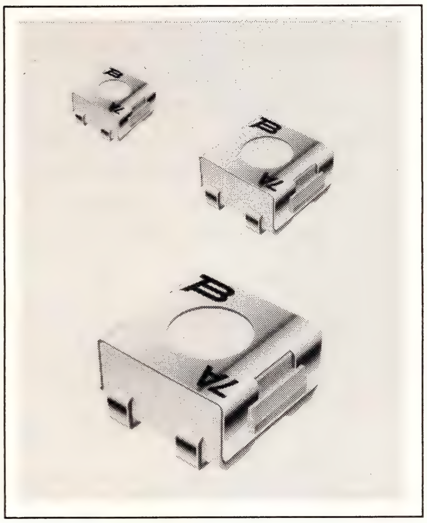
VC-7000 Series voltage-controlled crystal oscillators (VCXOs) are designed for high-speed, high-stability applications. The devices feature frequency stabilities of ±25 or ±50 ppm and aging of ±1 ppm per year.

Output frequencies for the oscillators range from 0.5 to 150 MHz. Output drive equals 10 TTL loads or 15 pF for HCMOS loads. Units operate from 5V, draw 35 mA, and offer control-voltage levels from 0.5 to 4.5V dc. Superimposed modulating frequency ranges as high as 10 kHz at the −3-dB points, and output linearity is better than ±10%. $15 (1000). Delivery, eight to 12 weeks ARO.

Raltron Electronics Corp, 2315 NW 107th Ave, Miami, FL 33172. Phone (305) 593-6033. FAX (305) 594-3973. Booth No. 2214.

Circle No. 407

Keyswitches



The Model 7914 keyswitch is a sealed surface-mountable unit that is compatible with all soldering processes. Available in top- or side-actuated versions, the switches measure 4.5×4.5×2.5 mm. The devices meet EIA/EIAJ/IPC/VRCI surface-mount outline dimensions and are compatible with popular pick-and-place equipment.

The normally open contacts in the 7914 are rated for 0.5 VA at maximum 16V and 100 mA. Contact resistance equals 100 mΩ max, and operating range spans −55 to +125°C. The switches come in J-hook and gull-wing terminal configurations. $1.03 (500).

Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (909) 781-5140. FAX (909) 781-5273. Booth No. 1840. **Circle No. 522**

Circuit analyzer

Model 545 tests boards without dc power applied, eliminating the need to determine a board's power requirements. It tests all components—passive, active, digital, or analog.

The analyzer applies an ac test signal to the device under test. A graph of the 545's display (with voltage on the X axis and current on the Y axis) shows the characteristic impedance of the device. A vertical line indicates a short; a horizontal line indicates an open. The unit includes a pulse generator and an automatic switcher. All cables are supplied. $2950.

B+K Precision, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448. FAX (312) 804-9425. Booth No. 1934. **Circle No. 523**

DIP switches

UD Series sealed DIP switches feature a 0.050-in. terminal spacing to conserve valuable pc-board space. The 8-position spst device uses copper alloy contacts with gold over nickel plating. Contacts are rated for 0.4 VA max at 20V ac or dc.

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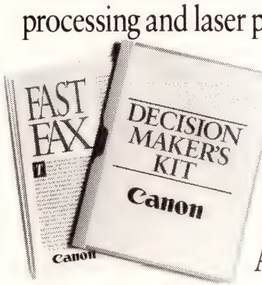

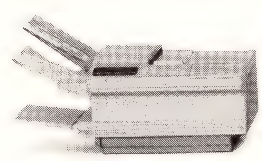

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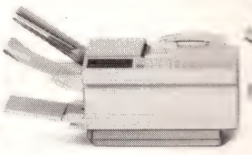

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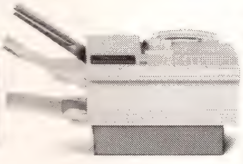

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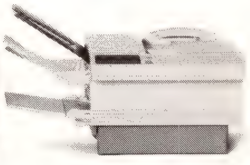

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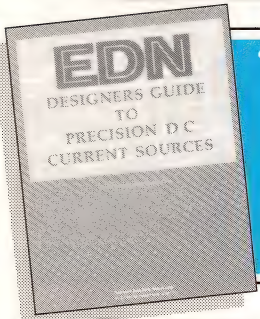

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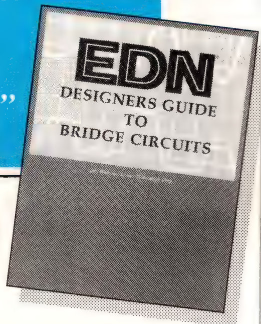

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DESIGNERS GUIDE
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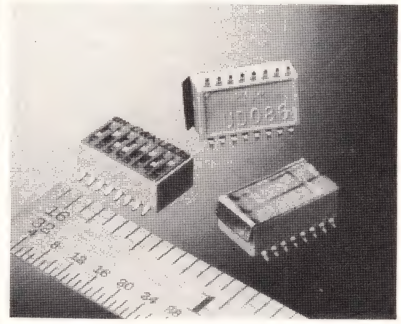

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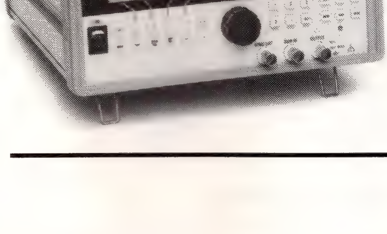

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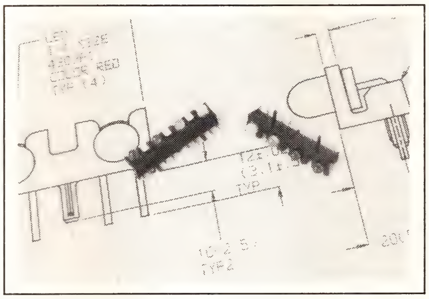

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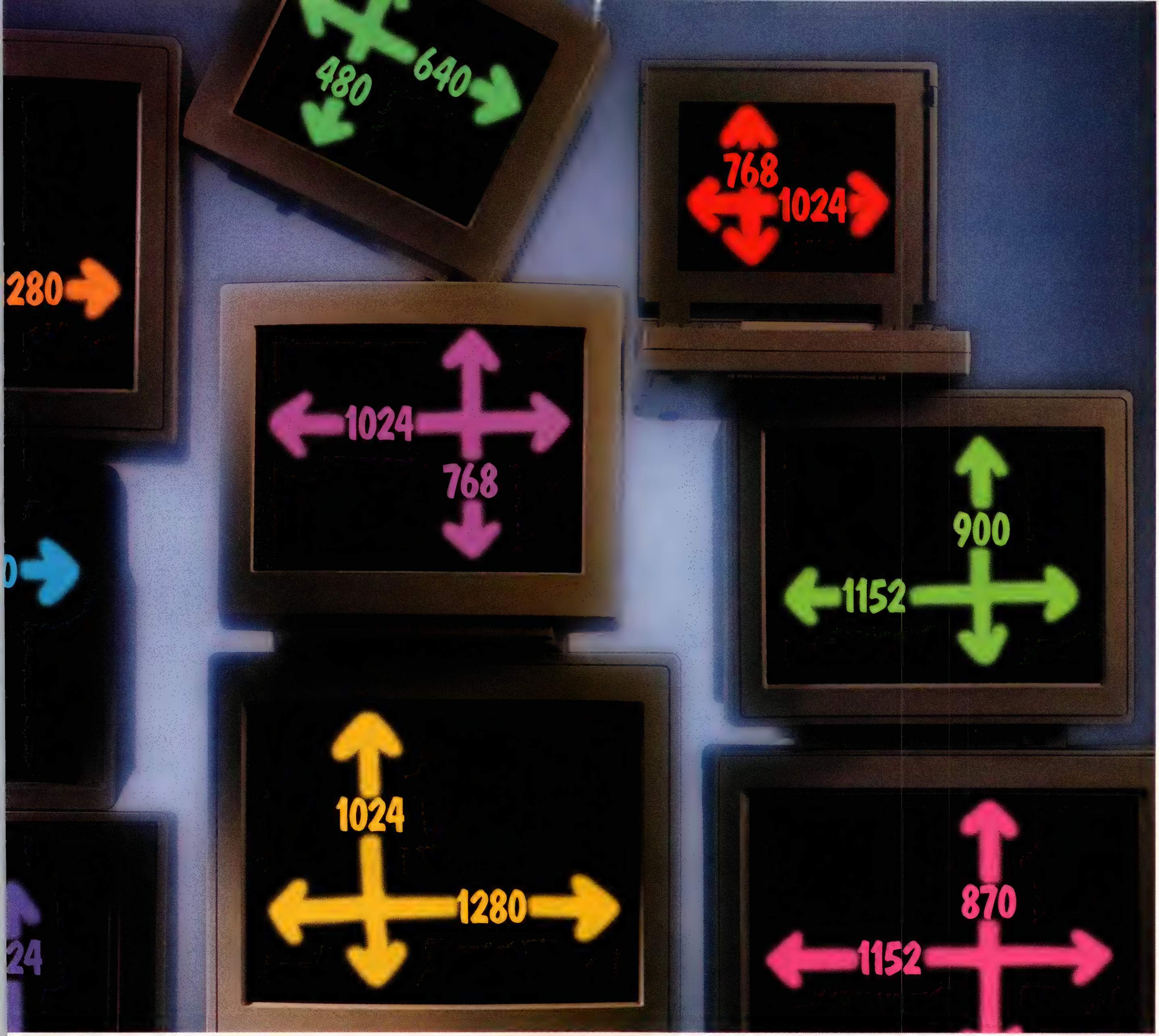

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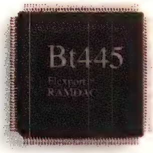

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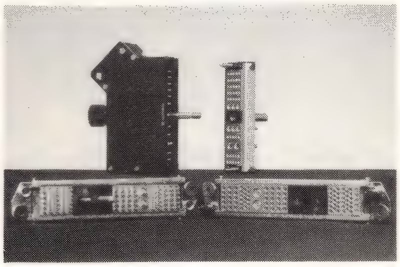

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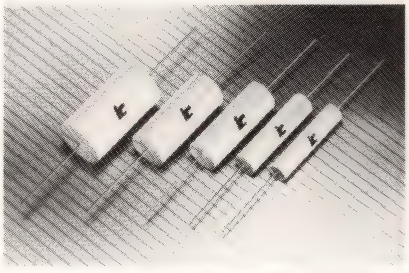

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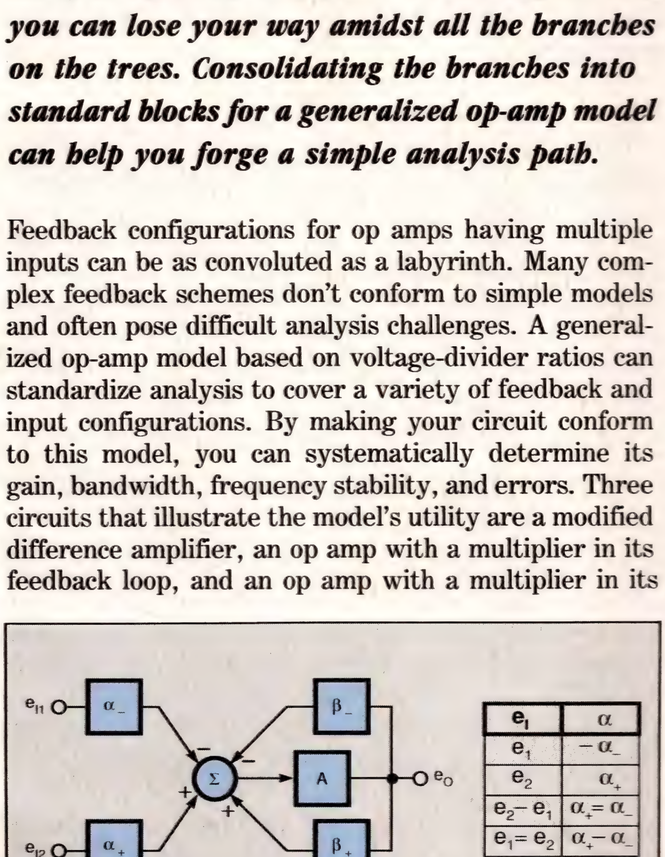
INNOVATOR

Generalized op-amp model simplifies analysis of complex feedback schemes

Jerald Graeme, Burr-Brown Corp

When attempting to find a path through a forest of complex op-amp feedback arrangements, you can lose your way amidst all the branches on the trees. Consolidating the branches into standard blocks for a generalized op-amp model can help you forge a simple analysis path.

Feedback configurations for op amps having multiple inputs can be as convoluted as a labyrinth. Many complex feedback schemes don't conform to simple models and often pose difficult analysis challenges. A generalized op-amp model based on voltage-divider ratios can standardize analysis to cover a variety of feedback and input configurations. By making your circuit conform to this model, you can systematically determine its gain, bandwidth, frequency stability, and errors. Three circuits that illustrate the model's utility are a modified difference amplifier, an op amp with a multiplier in its feedback loop, and an op amp with a multiplier in its feedforward path—a voltage-controlled lowpass filter.



e_I	α
e_1	$-\alpha_-$
e_2	α_+
e_2-e_1	$\alpha_+=\alpha_-$
$e_1=e_2$	$\alpha_+-\alpha_-$

Fig 1—A generalized model consolidates and directs all feedback and feedforward elements for a dual-input op amp towards a single summing junction.

Fig 1 shows the generalized model. The model represents the op amp and all possible feedback and input connections to it. It consolidates the sum and difference operations associated with the op amp's two inputs, e_{I1} and e_{I2}, into a single summing junction, Σ. (Note that the net op-amp input is e_I.) Composite elements for positive and negative feedback are consolidated in blocks β_+ and β_-, respectively. Similarly, the composite elements that represent the attenuation for positive and negative inputs to the op amp are consolidated in blocks α_+ and α_-. Block A represents the idealized op amp's gain, and e_O is the op amp's output.

The closed-loop gain (A_{CL}) of the generalized model is

$$A_{CL}=\frac{e_O}{e_I}=\frac{\alpha/\beta}{1+1/A\beta}=\frac{A_{CLi}}{1+1/A\beta}, \qquad (1)$$

where $\beta=\beta_--\beta_+$ and is the net amount of feedback for the model, and α and is the net feedforward attenuation for the inputs to the op amp (see table in **Fig 1**). The numerator α/β is the ideal closed-loop gain (A_{CLi}) when the open-loop gain ($A\beta$) is much larger than 1. The denominator of the equation, $1+1/A\beta$, is an expression that lets you determine the circuit's closed-loop bandwidth.

The model's closed-loop bandwidth is $BW=\beta f_C$, where f_C is the unity-gain crossover frequency of the op amp's forward gain (A). The generalized model lets you determine the gain for any error signals present at the op amp's input terminals. All op amps amplify these error signals by a gain of

$$A_{CLe}=\frac{1/\beta}{1+1/A\beta}.$$

You can apply this closed-loop error gain to any of the op amp's error signals, such as the input-offset voltage, input-noise voltage, and common-mode-rejection voltage.

The **Fig 1** model can accommodate one input to the op amp's positive input via the α_+ block and one input to the negative input via the α_- block. For multiple inputs, you must add α blocks. You determine the transfer function for each α block using superposition principles.

To illustrate the utility of the generalized model, we'll analyze some op-amp circuits having complex feedback and input configurations. **Fig 2a** depicts a configuration where the gain of an added op amp (IC_2) modifies the feedback of difference amplifier IC_1. Without the added op amp, the equal-valued resistors (R) set the difference-amplifier gain to 1. The fixed resistor values maximize the common-mode rejection ratio, and factory adjustments can trim the resistor ratios to within 0.002%.

IC_2 lets you change the circuit gain without affecting the difference amplifier's common-mode rejection ratio. You could analyze this circuit using A, α, β, and Σ blocks for each amplifier. Using the generalized model, however, you can simplify analysis by including IC_2 in the β_+ feedback path for IC_1. The fraction of the output voltage (e_O) fed back to IC_1's noninverting input is $\beta_+ = -\frac{1}{2}R_2/R_1$. Because there is no feedback to IC_1's inverting input, $\beta_- = 0$. The net feedback factor is $\beta = \beta_- - \beta_+ = R_2/2R_1$.

The equal values for the resistors surrounding the difference amplifier determine $\alpha_- = \alpha_+ = \frac{1}{2}$. In addition, the differential input signal is $e_I = e_{I2} - e_{I1}$. Substituting e_I, α, and β into the equation $A_{CLi} = e_O/e_I = \alpha/\beta$ yields

$$e_{Oi} = \frac{R_1}{R_2}(e_{I2} - e_{I1}),$$

where e_{Oi} is the ideal output signal. For the resistor values in **Fig 2a**, the addition of op amp IC_2 modifies the difference amplifier's ideal closed-loop gain (A_{CLi}) from 1 to 10.

You can analyze the circuit's frequency stability by examining the frequency-response curves for IC_1's open-loop gain, $|A_1|$, and the inverse of the net feedback factor, $1/\beta$, **(Fig 2b)**. The two curves intersect at frequency BW. For **Fig 2b**, the rate of closure—the difference in the slopes of the $|A_1|$ and $1/\beta$ curves where they intersect—is 20 dB/decade. This rate implies a 90° phase margin and excellent overall frequency stability.

The unity-gain crossover frequency for IC_2 is f_{C2}, and IC_2's net feedback factor is $\beta_2 = R_1/(R_1 + R_2)$. The rise in the circuit's $1/\beta$ curve at $\beta_2 f_{C2}$ shows the effect of IC_2's closed-loop bandwidth on stability. When $\beta_2 f_{C2} \geq 10BW$, the rise in the $1/\beta$ curve has negligible effect on stability. The typical crossover frequencies for the INA105 (IC_1) and OPA627 (IC_2) amplifiers are 2 and 16 MHz, respectively. Using $\beta = 0.05$ and $\beta_2 = 0.91$, $BW = \beta f_{C1} = 100$ kHz, and $\beta_2 f_{C2} = 14.6$ MHz. The effect of IC_2's closed-loop bandwidth on stability is negligible.

Two op amps can be better than one

You can also readily analyze the composite amplifier combination in **Fig 3a** using the generalized model. In this example, $A_{CL2} = (1 + R_4/R_3)$ is the closed-loop gain of IC_2, and A_1 is the open-loop gain of IC_1. The second amplifier modifies gain-block A of the generalized model so that $A = A_1 A_{CL2}$. The transfer function for the A block has two poles **(Fig 3b)**. One pole is due to the dominant pole for amplifier IC_1; the other pole is due to the closed-loop response of IC_2—$BW_2 = \beta_2 f_{C2}$. For frequency stability, the BW_2 pole must

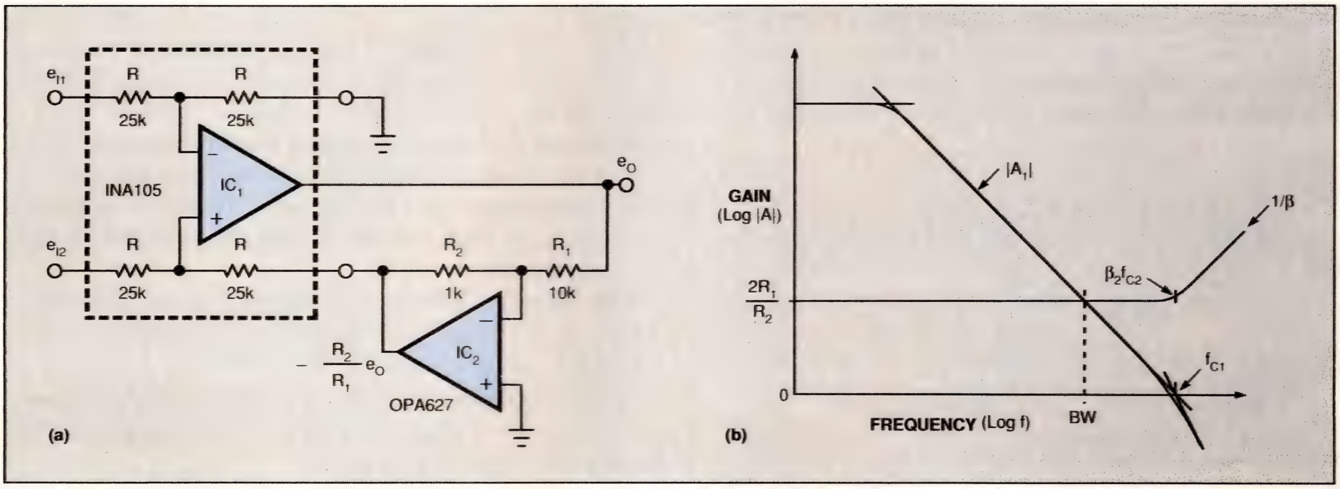


Fig 2—This modified difference amplifier (a) employs an op amp in the feedback to increase the gain without affecting common-mode rejection. For stability, the 1/β and |A| gain curves should intersect at a rate of closure of 20 dB/decade (b).

be considerably higher in frequency than the intercept point of the $|A_1|$ response curve and the $1/\beta$ response curve. For the circuit, $1/\beta = 1 + R_2/R_1$.

Introducing the second op amp reduces the error signals and increases the gain-bandwidth product of the circuit. The increase in loop gain due to IC_2 proportionally reduces the output error signal, $e_{0e}/A\beta$, caused by any error signal at IC_1's input terminals. The loop gain is the gain difference between the $|A|$ and $1/\beta$ curves. In addition, adding IC_2 increases the circuit's bandwidth from BW_1 to BW_2. For the resistor values in **Fig 3a,** the bandwidth increases by a factor of 10.

The generalized op-amp model also helps you analyze circuits having variable feedback elements. Variable feedback elements can include potentiometers, switches, and analog multipliers, all of which affect the magnitude and phase responses for $1/\beta$. The circuit in **Fig 4a** places an analog multiplier in the feedback loop of an op amp to create an analog divider. The divider's transfer function is $e_O = 10R_2e_I/R_1e_C$. To employ the generalized model, put the gain of the multiplier in the β block. Without the multiplier, the feedback factor for op amp IC_1 is $R_1/(R_1+R_2)$. The multiplier's transfer function, XY/10, scales e_O by $e_C/10$. Therefore, the net feedback factor for the model, which takes into account e_C, is

$$\beta = \frac{e_C R_1}{10(R_1+R_2)}.$$

Fig 4b illustrates the effect of the e_C variable control signal on the circuit's bandwidth and stability. The control-signal voltage moves the intercept point for the $1/\beta$ curve over the full range of the $|A|$ curve. When e_C is 0V, β is zero, and the op amp operates open loop. When e_C is 10V, the multiplier gain is 1,

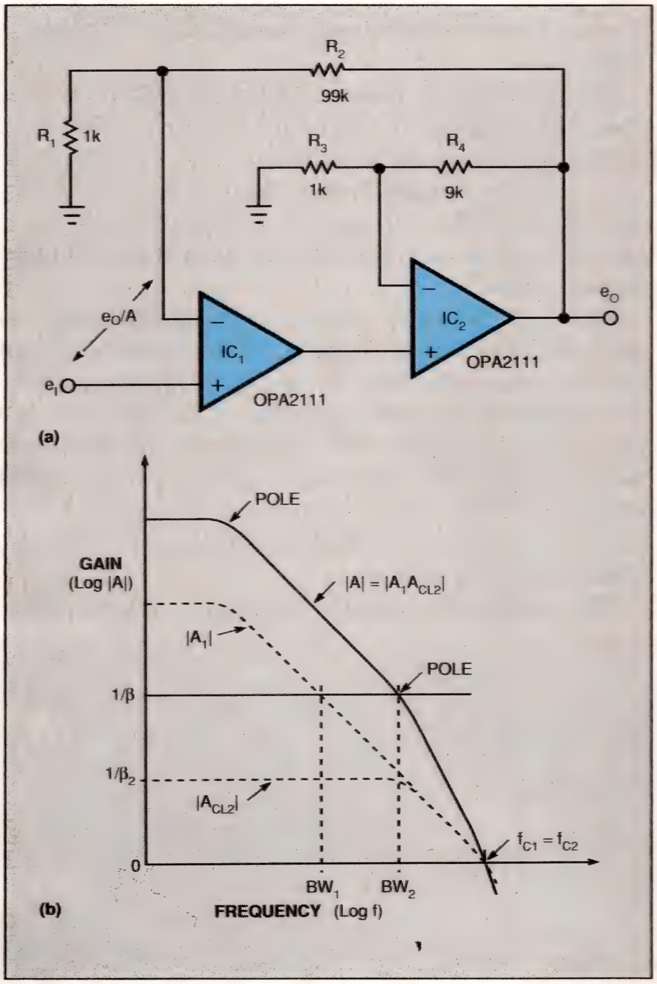


Fig 3—You can increase the net open-loop gain and closed-loop bandwidth by placing an additional op amp in the forward gain path (a). The closed-loop response of the additional amplifier places a second pole in the A gain block (b), which determines the circuit's stability.

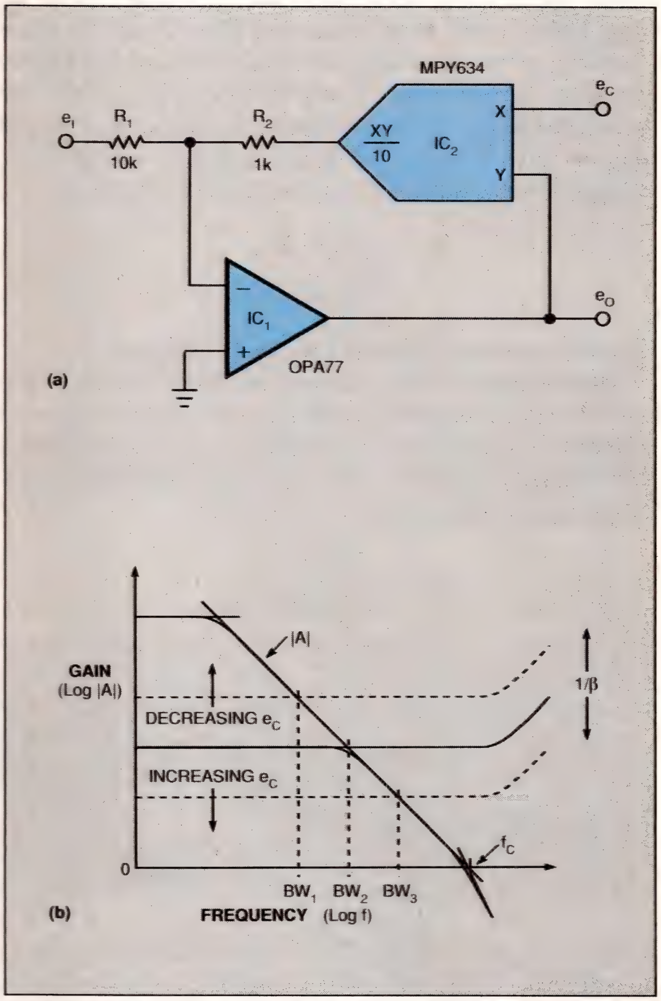


Fig 4—The addition of a multiplier in the feedback of an op amp lets you divide inputs from two signal sources (a). The net feedback factor β varies with control voltage e_C (b), so you must analyze the circuit's stability over the entire control-voltage range.

and the device can be replaced with a short circuit. Because the intercept point varies, you must pay close attention to the rate of closure of the two curves over the entire control-voltage range.

A pole in the multiplier's frequency response causes the 1/β curve to rise, as **Fig 4b** shows. To maintain circuit stability, the op amp must have a dominant pole so the moving intercept point always occurs on the flat portion of the 1/β curve. The OPA77 op amp's 0.6-MHz bandwidth and the MPY634 multiplier's 16-MHz bandwidth make the devices good choices to ensure the circuit's frequency stability. For the component values in **Fig 4a,** β varies from 0.00091 to 0.091 as e_C varies from 0.1V to 10V. The circuit bandwidth changes proportionally from 550 Hz to 55 kHz.

To use the generalized model for circuits having multiple inputs to the op amp, you must apply superposition principles. **Fig 5a** shows an example where three input signals connect to the inverting input of an op amp through different networks. **Figs 5b** and **5c** show redrawn versions of the circuit that let you use superposition to determine α and β, respectively, for the generalized model. To determine β, use e_O as a signal source, and set all of the input sources to ground. Under these conditions, the net feedback factor is

$$\beta = \frac{R_1 \| R_2 \| R_3}{R_1 \| R_2 \| R_3 + R_F}.$$

For the resistor values in **Fig 5a,** β = 0.009.

To determine α for a particular input, set all of the signal sources except the input under consideration to ground. To determine α_1 for input-source e_1, calculate the voltage divider to the op amp's inverting input when e_2, e_3, and e_O are set at ground:

$$\alpha_1 = \frac{R_F \| R_2 \| R_3}{R_F \| R_2 \| R_3 + R_1}.$$

For the resistor values in **Fig 5a,** $\alpha_1 = 0.9$. Using the same approach to calculate the αs for the input sources at e_2 and e_3 yields $\alpha_2 = 0.09$ and $\alpha_3 = 0.009$.

Although the attenuation (α) block for each input source is different, the circuit's bandwidth and stability considerations are the same for all input sources. The reason is that the denominator for A_{CL} in **Eq 1,** which is $1 + 1/A\beta$, is the same for all input sources and doesn't depend on α. The circuit's bandwidth is $BW = \beta f_C$ for all input sources.

Increasing the number of op-amp inputs constricts the bandwidth of the circuit, however. For the **Fig 5** example, if e_3 is the only input source, the net feedback factor is $\beta = R_3/(R_3 + R_F) = 100\ k\Omega/(100\ k\Omega + 100\ k\Omega) = 0.5$. The OPA111 has a unity-gain cross-over frequency (f_C) of 2 MHz, so the circuit bandwidth is $BW = 0.5 \times 2\ MHz = 1\ MHz$. The addition of the other two input sources to the circuit reduces the net feedback factor to β = 0.009. Therefore, the added input sources decrease the circuit bandwidth to 18 kHz—a factor of 55.

The different α blocks determine different ideal closed-loop gains for each input source. The ideal closed-loop gain expression is $A_{CLi} = \alpha/\beta$. Therefore, the ideal closed-loop gain for the input sources at e_1, e_2, and e_3 are −100, −10, and −1, respectively. However, the closed-loop bandwidth is still 18 kHz for all three input sources.

Finally, look at an op-amp configuration that employs multiple feedback paths. **Fig 6** depicts a circuit that has feedback from the op amp's output and from the output of an added multiplier. The multiplier is a gain block in series with the circuit's forward gain path and alters the net forward gain as well as the net feedback factor. The multiplier and the resistor feedback convert the circuit from an integrator to a voltage-controlled lowpass filter.

The multiplier's transfer function is XY/10. When

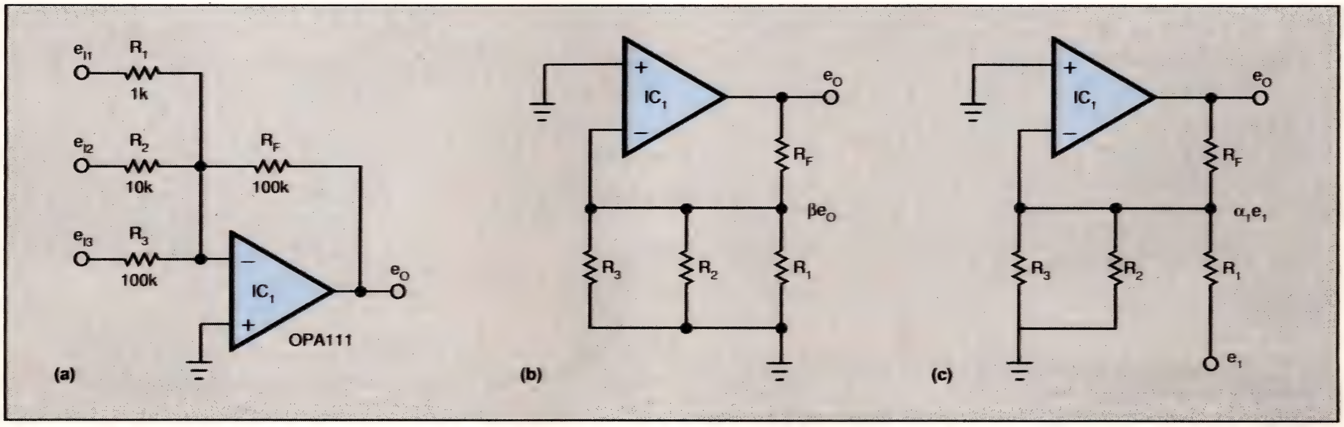


Fig 5—To determine β and α for op-amp configurations having multiple inputs (a), you must apply superposition principles. The redrawn models let you determine β (b) and α (c) using parallel equivalent resistors for the respective voltage dividers.

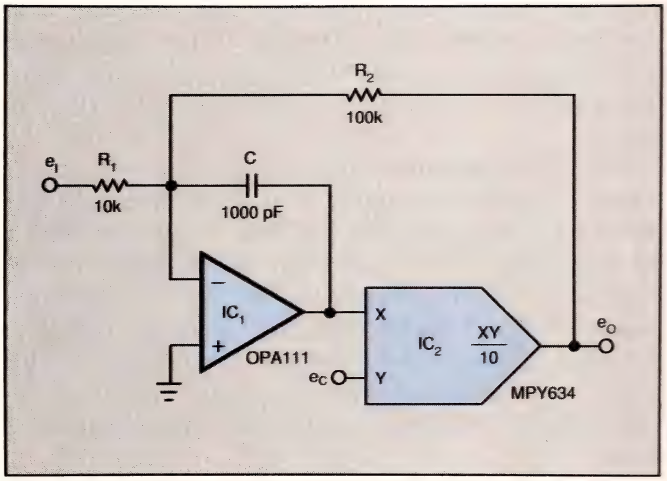


Fig 6—Adding a multiplier in the feedforward path changes a basic integrator circuit into a voltage-controlled lowpass filter. This circuit shows how you can use the generalized model to analyze an op-amp configuration that employs multiple feedback paths.

control-voltage e_C is 10V, the multiplier acts as a short circuit. Under this condition, resistor R_2 and capacitor C feedback produce a standard lowpass filter having a pole frequency, f_P, at $1/2\pi R_2C$. When e_C is less than 10V, the attenuation to the voltage at pin X on the multiplier is $e_C/10$. The attenuation reduces the voltage driving R_2, which in turn reduces the current feedback to the op amp's summing junction. The effect is the same as increasing R_2's value to $10R_2/e_C$. The increase in the effective resistance changes the lowpass-filter pole frequency to $e_C/20\pi R_2C$.

To analyze this circuit's performance using **Eq 1** for the generalized model, you must determine A_{CLi}, A, and β. At very low frequencies, the closed-loop gain is $-R_2/R_1$, because the capacitor has no effect. At higher frequencies, the voltage-controlled corner frequency determines the closed-loop roll-off. Therefore, the closed-loop gain is

$$A_{CL} = \frac{e_O}{e_I} = \frac{A_{CLi}}{1+1/A\beta} = \frac{-R_2/R_1}{1+s(10R_2/e_C)C}.$$

Both the op amp and the multiplier determine the forward gain of the model, so $A=A_1e_C/10$. The net feedback factor, β, depends on two feedback paths. **Fig 7a** depicts the feedback model for the **Fig 6** circuit. The β_C and β_R blocks represent the feedback to the op amp's inverting input through the capacitor and resistor (R_2), respectively. The net feedback factor is

$$\beta = (10/e_C)\beta_C + \beta_R.$$

The voltage fed back through the capacitor precedes the attenuation caused by the multiplier. Therefore, β_C is magnified by $10/e_C$, because the voltage at the multiplier's input is $(10/e_C)e_O$. **Fig 7b** shows the 1/β and |A| curves for the **Fig 6** circuit. The dashed curves show how the two curves change with variations in e_C. The 1/β and |A| curves move up and down

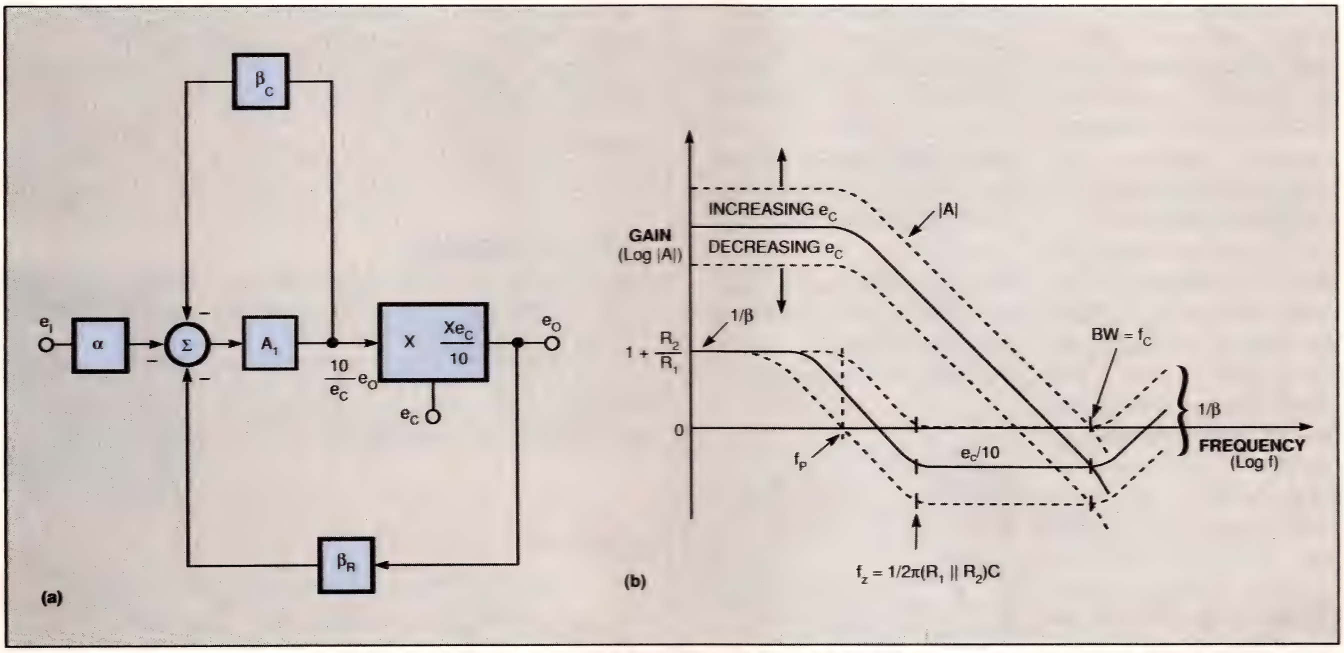


Fig 7—The block diagram for the voltage-controlled lowpass filter reveals the multiplier's effect on the feedforward and feedback paths (a). When analyzing the circuit's stability, you must consider the variations in the |A| and 1/β curves over the entire control-voltage range (b).

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CIRCLE NO. 22

together, so the intercept point and corresponding bandwidth remain fixed. The rise in the $1/\beta$ curve at high frequencies is due to the bandwidth of the multiplier and determines the rate of closure for the two curves.

The circuit demonstrates a condition not usually found in op-amp configurations. When the multiplier provides attenuation, the feedback is greater than 1 at high frequencies. Generally, the feedback cannot exceed 1, but in this case the multiplier attenuation causes a signal larger than the e_O output signal to feedback through the capacitor. Therefore, the $1/\beta$ curve drops below the unity-gain axis. The circuit remains stable, however, because the intercept point is fixed.

The shape of the $1/\beta$ curves indicate the frequencies at which either of the two feedback paths dominate. Feedback is primarily through the β_R block in the flat portion of the $1/\beta$ curve labeled $1+R_2/R_1$. Feedback through the β_C block begins at the pole located at $f_P=20\pi R_2C$ and causes the slope of $1/\beta$ curve to decrease at 6 dB/octave. Feedback is primarily through the β_C block in the flat portion of the $1/\beta$ curve labeled $e_C/10$. The curve before this flat portion levels off at the zero located at $f_Z=1/2\pi(R_1 \parallel R_2)C$, where $R_1 \parallel R_2$ is the equivalent parallel resistance of R_1 and R_2. EDN

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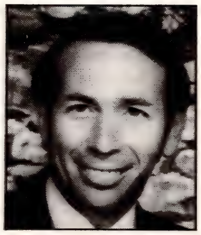
Author's biography



Jerry Graeme, a prolific contributor to EDN, manages instrument-components design for Burr-Brown Corp in Tucson, AZ. At Burr-Brown, he has personally designed many analog ICs. He holds a BSEE from the University of Arizona and an MSEE from Stanford.

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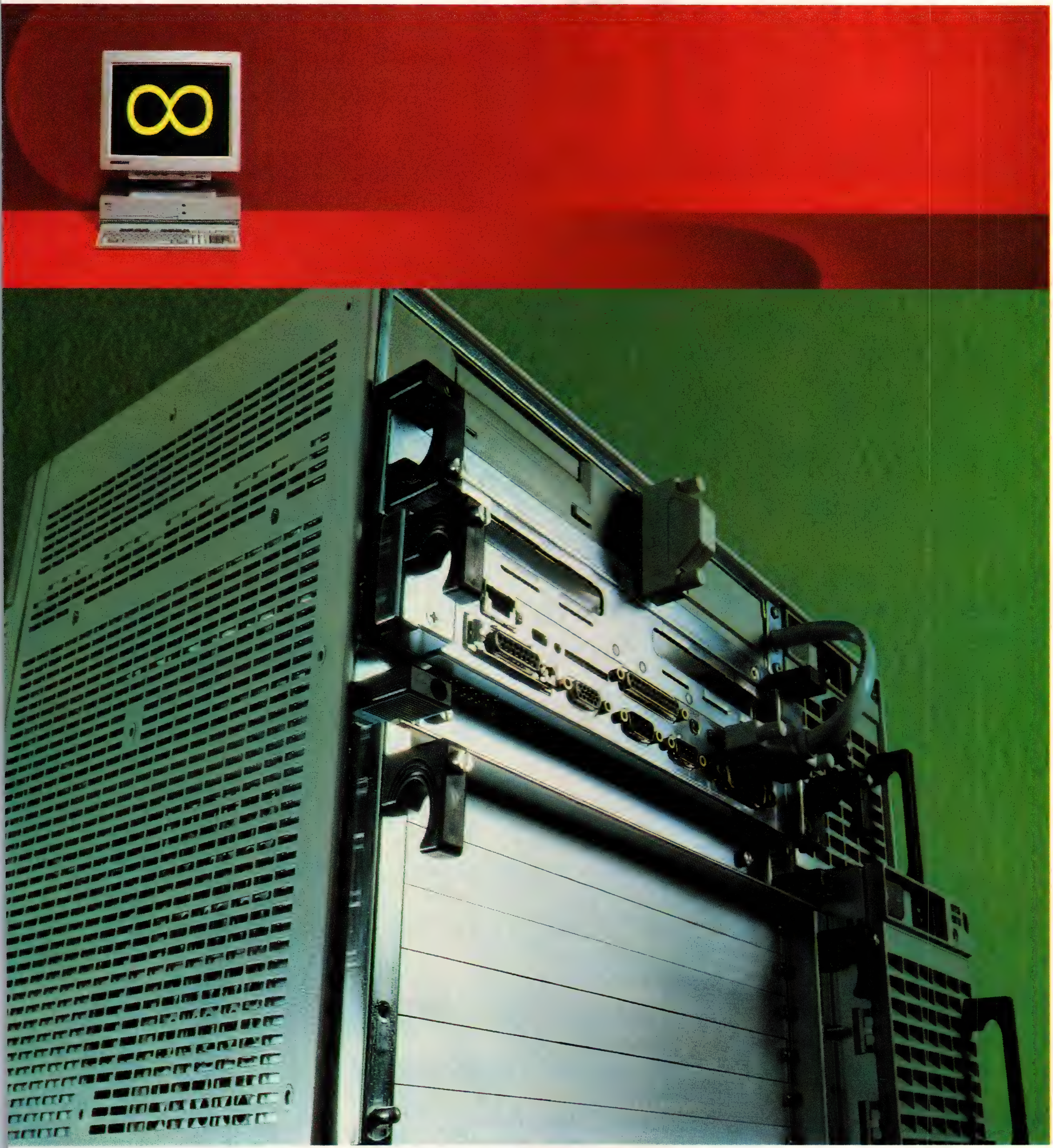

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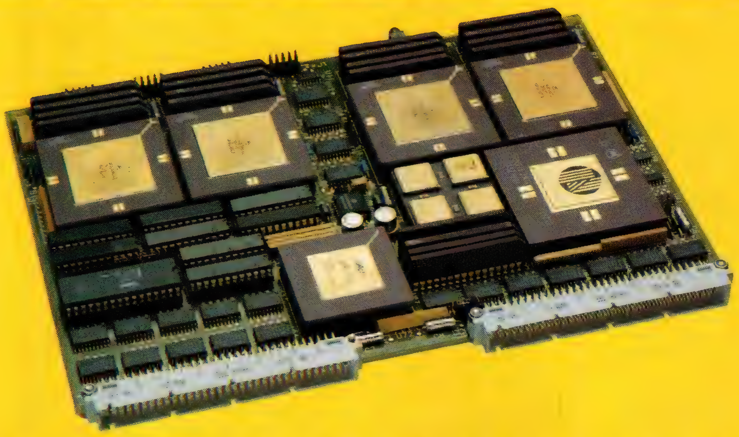

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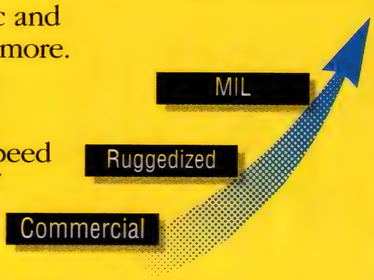

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CIRCLE NO. 96

Graft Windows programs to your custom software and reduce your workload

Bill Tolson, Hewlett-Packard Co

Combine Windows programs with your own software to save time and effort when building complex custom systems. Specific examples include using the spreadsheet Excel for data analysis and graphing, or, for drawing and graphing, using word-processor Word for Windows.

Using the facilities of standard Windows programs can greatly reduce the amount of custom software you must write. This article will demonstrate that a test engineer can devise a complete custom test program using only Excel and Word for Windows.

When compared with other operating systems, Windows eases the combining of standard programs with software you have written. Using other operating systems, you have to fire up each standard program as you need it, and then pass data between programs via shared files. Under Windows, multitasking programs work together simultaneously. Windows programs pass data and commands back and forth using the unique Windows facility called DDE (dynamic data exchange).

For a test engineer using standard Windows programs for displaying data, two problems remain: acquiring data from instruments and submitting the data to the Windows programs for processing.

The solution to these two problems involves another interesting Windows facility, the DLL (dynamic link library). DLLs are special library programs that let Windows programs share code and resources (**Fig 1**). A DLL is an executable module containing functions that Windows programs can call at will to perform useful tasks.

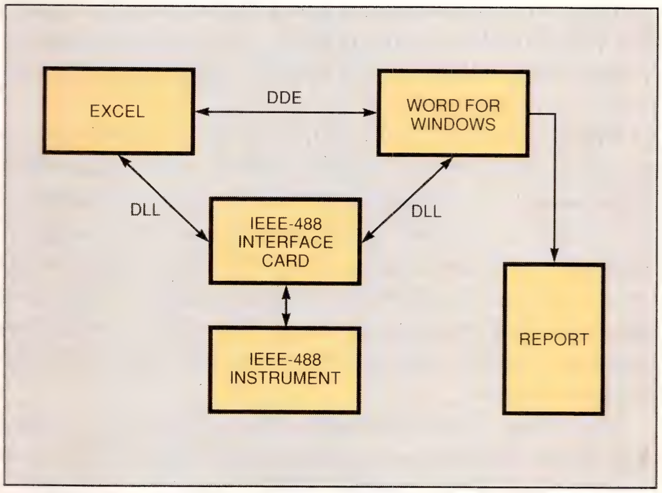

Fig 1—The Windows' DLL feature lets programs share code and resources.

Do not confuse a Windows DLL with a DOS .LIB library file. The difference between a .LIB library file in DOS and a DLL file in Windows is that a .LIB file comprises object code linked into a program file at link/compile time. In DOS programs, each DOS .EXE program gets its own copy of each .LIB file, greatly increasing the size of each program.

A DLL file comprises object code linked *dynamically* into a Windows program (.EXE file) only at run-time as necessary. DLLs decrease the size of a Windows .EXE file because the DLLs are loaded only as needed. That is, a Windows program can do on the fly what linkers do statically to conventional programs.

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #498Z."

Another plus of a DLL is that several executing Windows .EXE programs can use the same DLL. Luckily, many of the new Windows programs can call *foreign* DLLs, not just their own.

So how does a DLL solve the problem? Newer interface cards for PCs, such as the HP 82335B IEEE-488 for Windows, come with their own DLL. The 82335B's DLL is a DOS command-library program rewritten in DLL format. When the DLL receives an IEEE-488 command, the DLL provides the detailed, arcane instructions for the procedure the interface card executes.

Normally, a test engineer would use the interface card's DLLs in conjunction with his own custom Windows programs. But an Excel macro can also invoke a DLL's function; in Word for Windows, Word Basic can call external DLLs. Thus, the test engineer can simply write Excel macros or Word Basic programs to acquire data.

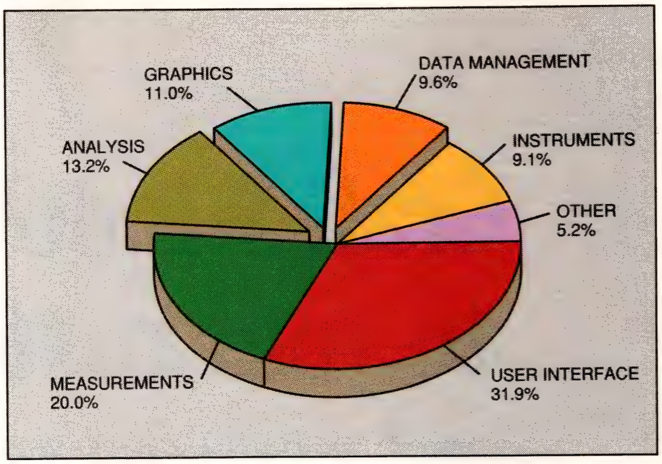

Fig 2—This breakdown of a standard instrument-control program is representative of most such programs. Notice that an average program requires you to spend one-third of the your programming time on code that analyzes the data, performs graphics routines, manages the data, and presents the data.

The benefits

Why should you learn a new programming language for Excel macros or Word Basic when you are already comfortable with a programming language? The answer is, "It depends."

Fig 2 presents a breakdown of a standard instrument-control program. This particular breakdown is representative of most instrument-control programs. Note that an average program requires you to spend one-third of your programming time on code that analyzes the data, performs graphics routines, manages the data, and presents the data. Note that this fraction does not include time spent formatting the results for a formal report.

By pulling the data directly into a spreadsheet, word processor, database, or some other program, you save a great deal of the one-third time figure for managing, analyzing, and presenting the data. The main argument is that standard programs perform various tasks, such as data analysis or graphics, very well. And why duplicate these abilities in your own program when they are already available?

If you don't require high-speed communications (>200-kbyte/sec transfers) and need to deliver the results in a presentable document, or, if you'll be performing simple, repetitive data-acquisition tasks, then instrument control from Windows programs is a good alternative to writing a custom program.

Testing high-reliability components and subassemblies provides an example on which to test this method. Suppose that the tests require you to characterize, for your records or your customers, the parts and then prepare a final data sheet for each serial-numbered component.

The data is first collected and analyzed by hand and then submitted in a typewritten data sheet. Now, a macro running in Excel can acquire the data directly from the device into a spreadsheet, analyze it, and then direct it to a preformatted data sheet for printing in Word for Windows. This example includes collecting a number of readings from a thermistor, calculating various statistics for the readings, and finally creating a bar chart showing the data. The bar chart and statistics then go into a preformatted data sheet in Word for Windows using the DDE protocol.

The examples use Windows 3.1, Excel 3.0, Word for Windows 2.0, and the HP 82335B IEEE-488 for Windows interface card. The interface card controls an IEEE-488-compatible digital voltmeter (DVM).

The code for the actual DLL declarations and communications with the IEEE-488 device in **Listing 1** is pretty straightforward. The shaded area in the spreadsheet listing is all that's necessary for communication with IEEE-488 devices.

When accessing a foreign DLL from Excel, on the other hand, you must first register the DLL with the macro. The REGISTER command accomplishes this operation. The specific command sequence is

```
=REGISTER([name of the DLL],[name of the
   procedure in the DLL],[the data type]).
```

Thus, in the first REGISTER statement, the name of the external DLL is "HPIB.DLL."

Because DLLs usually contain many different procedures, you must REGISTER each procedure you will be using in the DLL. The name of the first procedure in the first REGISTER statement is "HpibOpen." The specifics of the available procedures in any DLL you are using should be in the interface card's manual.

In addition, you will also find definitions of the interface card's data types in its manual. Once you have the card's data types, you will need to convert them to something Excel understands. Appendix A in the Microsoft Excel Function Reference explains the various data types Excel understands. The DEFINE.NAME command immediately below each REGISTER statement creates a name for each procedure. Later on, this name makes using the CALL statements easier.

The shaded area in the "B" column of **Listing 1** performs the actual communication with the IEEE-488 devices. The command statement in line B9 executes the HpibOpen procedure from the interface card's DLL and places the so-called "handle" returned in cell C10. "Handle" is a Windows term that refers to the offset into a table in memory. If you have some object's handle, you can always find the actual address of that object at any point in time. Windows needs this indirect memory-allocation scheme because it moves chunks of memory around while multitasking. This handle will figure in the rest of the procedures. The statement in line B10 simply converts the handle in C10 into a numeric value and places it in cell C11.

The command statement in line B11 resets the IEEE-488 bus. The command in line B12 sends the string found in cell C13 to the IEEE-488 device. In this case, the string changes the measurement mode to measure ohms.

Listing 1—Excel macro

	A	B	C
1	=RUN(A5)	=DISPLAY(FALSE)	
2	=RUN(B1)	=ECHO(TRUE)	
3	=RETURN()	=INPUT("Enter the rated value of the part:",1)	
4		=INPUT("Enter the tolerence:",1)	
5	DefineFunctions	=B3-(B4*B3)	
6	=REGISTER("HPIB.DLL","HpibOpen","FJF")	=B3+(B4*B3)	
7	=DEFINE.NAME("HpibOpen",A6,1)	=INPUT("How many measurements would you like to make?",1)	
8	=REGISTER("HPIB.DLL","HpibReset","IIJ")	=B7-1	
9	=DEFINE.NAME("HpibReset",A8,1)	=SET.VALUE(C10,CALL(HpibOpen,7,C10))	
10	=REGISTER("HPIB.DLL","HpibOutputs","IIJCI")	=SET.VALUE(C11,CODE(C10))	
11	=DEFINE.NAME("HpibOutputs",A10,1)	=CALL(HpibReset,C11,7)	
12	=REGISTER("HPIB.DLL","HpibEnters","FIJFM"	=CALL(HpibOutputs,C11,722,C13,3)	
13	=DEFINE.NAME("HpibEnters",A12,1)	=FOR("COUNT",0,B8,1)	OHM
14	=REGISTER("HPIB.DLL","HpibClose","II")	=SET.VALUE(C14,CALL(HpibEnters,C11,722,C14,100))	
15	=DEFINE.NAME("HpibClose",A14,1)	=SET.VALUE(OFFSET(D1,COUNT,0),VALUE(CLEAN(C14)))	
16	=REGISTER("HPIB.DLL","HpibEnter","FIJF")	=NEXT()	
17	=DEFINE.NAME("HpibEnter",A16,1)	=CALL(HpibClose,C11)	
18	=RETURN()	=AVERAGE(D1:D100)	
19		=MEDIAN(D1:D100)	
20		=MAX(D1:D100)	
21		=MIN(D1:D100)	
22		=SELECT(D1:OFFSET(D1,B8,0))	
23		=NEW(2)	
24		=GALLERY.COLUMN(2,FALSE)	
25		=COPY.PICTURE(1,1)	
26		=EXEC("C:\WINWORD\WINWORD.EXE C:\WINWORD\TEST	
27		=INITIATE("WINWORD","C:\WINWORD\TEST3.DOC")	
28		=POKE(B27,"VALUE",B3)	
29		=POKE(B27,"TOL",B4)	
30		=POKE(B27,"HIGH",B6)	
31		=POKE(B27,"LOW",B5)	
32		=POKE(B27,"MAX",B20)	
33		=POKE(B27,"MIN",B21)	
34		=POKE(B27,"AVG",B18)	
35		=POKE(B27,"MED",B19)	
36		=TERMINATE(B27)	
37		=SEND.KEYS("%ommacro3{ENTER}",TRUE)	
38		=DISPLAY(TRUE,)	
39		=RETURN()	

Listing 2—Word for Windows macro

```
Sub MAIN
LineDown 21
EditPaste
FilePrint .Type = 0, .NumCopies = "1", .Range
= 0, .From = "", .To = "", .PrintToFile = 0,
\
.Collate = 1, .FileName = ""
End Sub
```

The macro now sets up a For/Next loop beginning in line B13. Line B13 sets up a loop counter named "COUNT" with an initial value of 0 and a maximum reference using the value returned in cell B8. Lastly, the statement sets a loop increment of one. In line B14, the CALL command accepts the reading from the DVM and places the reading in cell C14.

To format the reading properly, the SET.VALUE command that begins line B14 changes the string in C14 to a value. Then, the command line in B15 shifts the data into column D, one datum at a time, while converting the data to numbers.

After taking all of the data, the macro uses the HpibClose command in line B17 to free the interface card for possible use by another program.

Now that all the data has been funneled into the spreadsheet, the macro runs the statistics routines, creates the graph, and activates Word for Windows beginning in line B26. The macro loads a Word for Windows, preformatted data sheet and inserts the data into various sections of the data sheet using POKE commands.

The command in line B37 of the Excel macro activates another macro in Word for Windows called "macro3." This Word for Windows macro centers the chart and prints out the final data sheet. Check **Listing 2** for macro3's code.

Author's biography

Bill Tolson is a product-marketing engineer for Hewlett-Packard's VXI Systems Division in Loveland, CO. Bill has been with HP for 11 years. In the past, he has helped to develop a PC-to-IEEE 488 interface and a high-performance measurement coprocessor. He obtained a BS from El Camino College, California State University in Dominguez Hills, CA. In his spare time he enjoys hiking, writing, and programming.

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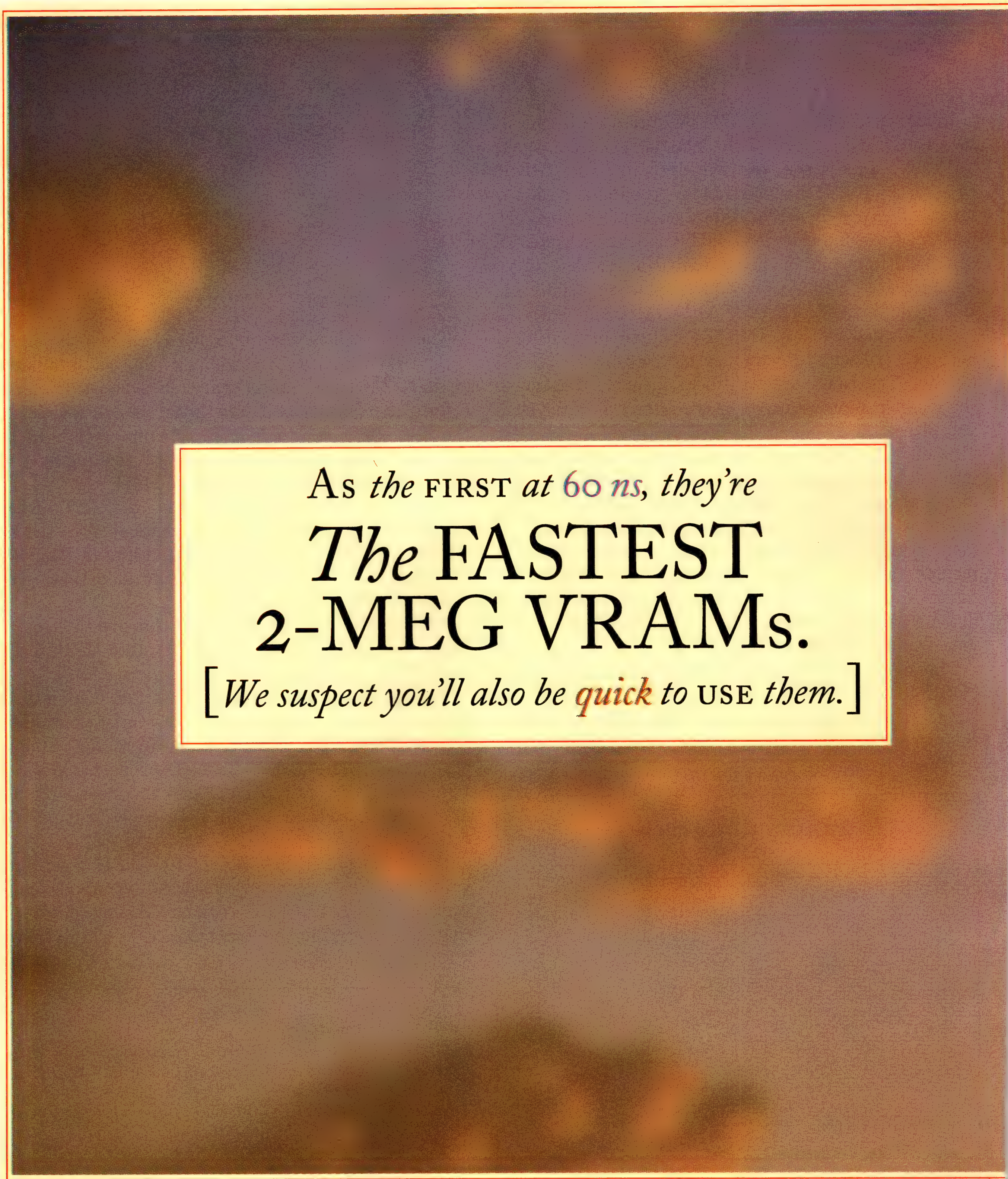

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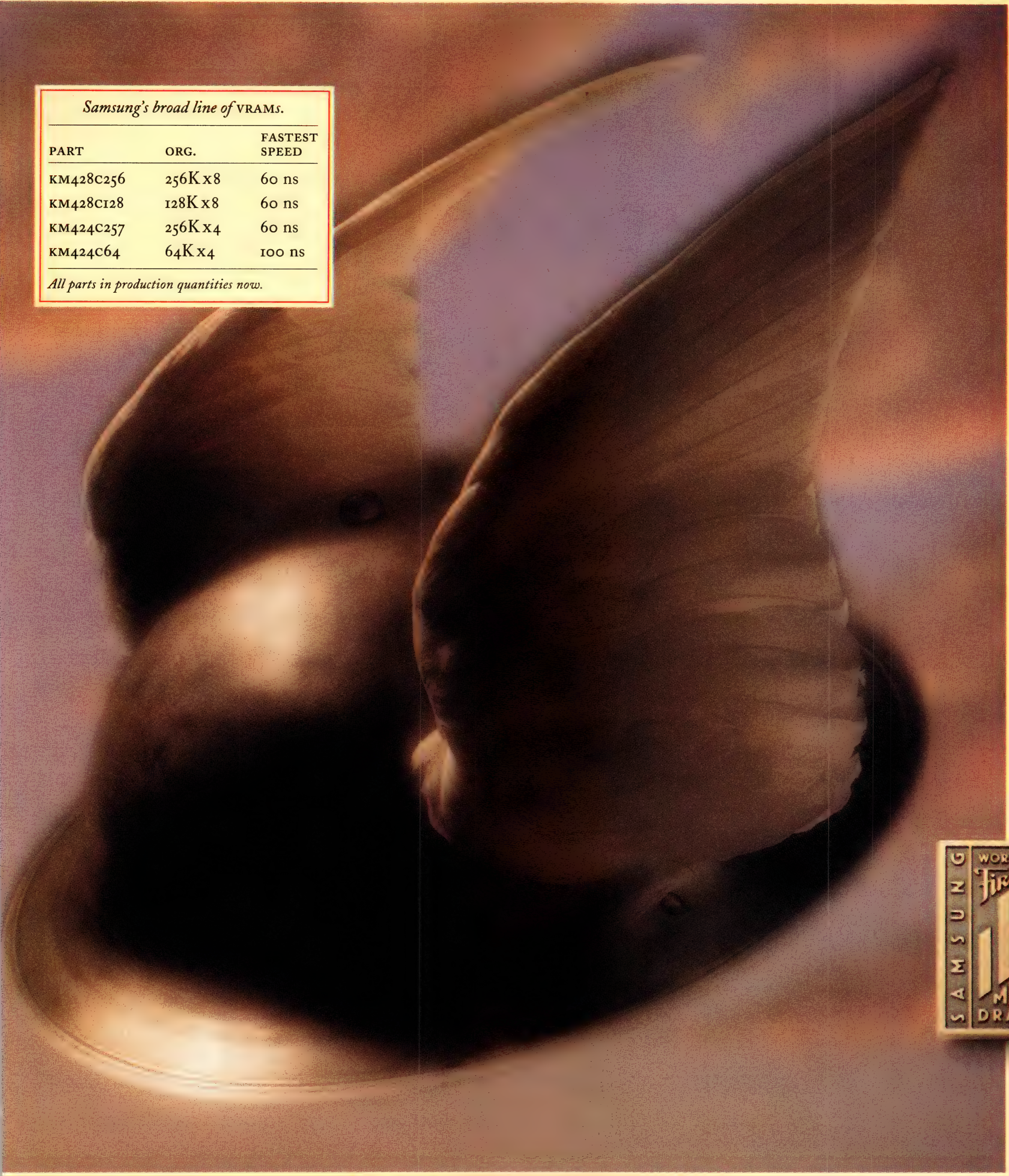

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MP8798	10 bit	1 MHz	50 mW	4	5 V	13.83
MP8799	10 bit	1 MHz	50 mW	8	5 V	15.44
MP8775	8 bit	20 MHz	125 mW	1	5 V	6.44
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MP87L84	10 bit	2 MHz	50 mW	1	3.3 V	13.60
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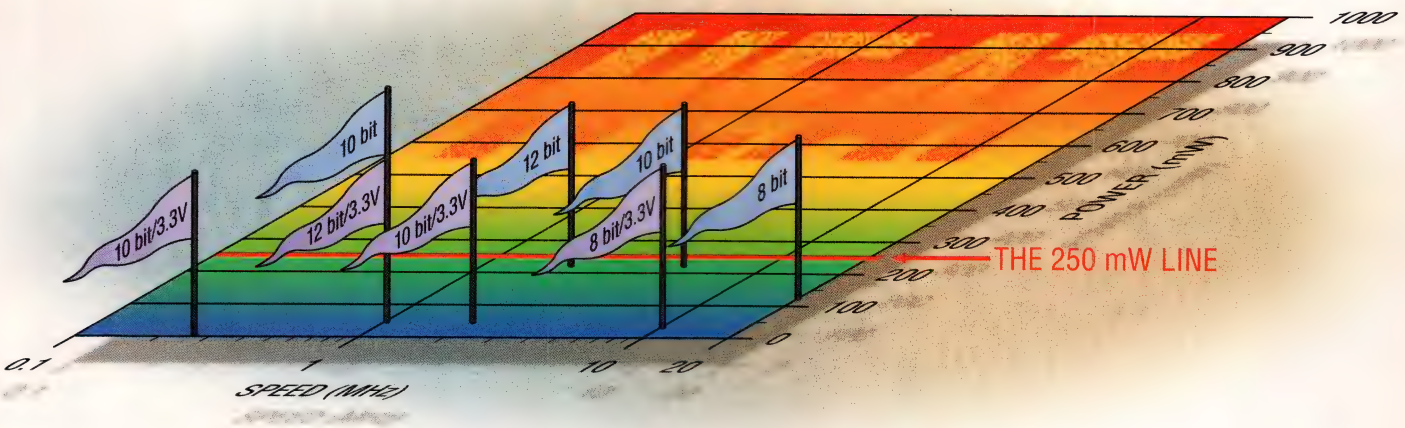

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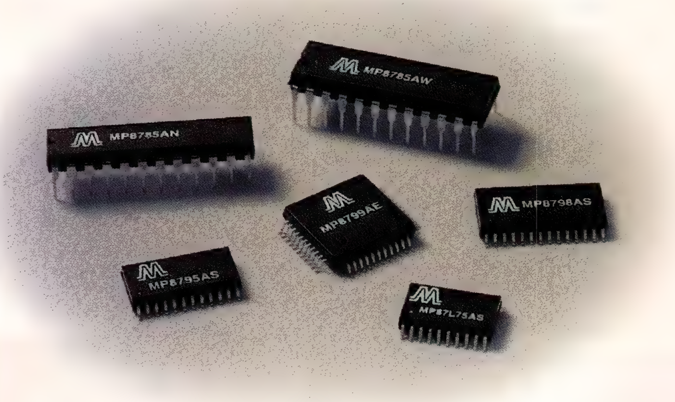

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DESIGN NOTES

Low Parts Count DC/DC Converter Circuit With 3.3V and 5V Outputs – Design Note 69

Ron Vinsant

This Design Note describes a simple low cost dual output step-down converter circuit based on the LT1076 five terminal switching regulator.

Performance

Input voltages can range from 8V to 30V. The load range on the 5V is 0.05A to 0.5A while the 3.3V load range is 0.1A to 1A. The circuit is self-protecting under no load conditions; it will "burp" in the same fashion as many off-line flyback power supplies.

Output voltage regulation is excellent. Over all load and line conditions, including cross regulation, the 3.3V output varies from 3.25V to 3.27V. The 5V output varies from 4.81V to 5.19V under the same conditions.

In a typical application of 0.5A on the 3.3V and 0.25A on the 5V, efficiency is typically 76%. With an input voltage of 30V and full load, the efficiency drops to 66%. In normal operating regions efficiency is always better than 70%.

The 5V ripple is less than 75mV and the 3.3V ripple less than 50mV over all line and load conditions.

This design can help save both parts and cost by the elimination of a second regulator. Only a few additional parts are required to make the second output. They are: two resistors, a Schottky diode, a small ceramic capacitor and a filter electrolytic; only 5 additional components! The normal single winding inductor has one small winding added to create the additional output.

The circuit has been built in our lab and has only been evaluated for room temperature performance. No stability analysis has been done.

Performance Table

V_{IN}	V_{OUT}, OUTPUT 1 (5V)	V_{OUT}, OUTPUT 2 (3.3V)
	@ $I_{OUT} = 0.4A$	@ $I_{OUT} = 1A$
8V	4.81	3.26
30V	5.07	3.26
	@ $I_{OUT} = 0.05A$	@ $I_{OUT} = 1A$
8V	5.14	3.25
30V	5.19	3.25
	@ $I_{OUT} = 0.4A$	@ $I_{OUT} = 0.1A$
8V	4.81	3.26
30V	5.02	3.27
	@ $I_{OUT} = 0.05A$	@ $I_{OUT} = 0.1A$
8V	5.07	3.26
30V	5.11	3.26

Inductor

The inductor is based on a EP-13 ferrite core which is available from a number of vendors. In our breadboard we used a Ferroxcube core in 3C81 material gapped to 6 mils (center gap). The 3.3V winding is 22 turns of #25 AWG while the 5V winding is 13 turns of #28 AWG. Any magnetics vendor should be able to wind this device. The inductor has only a 14°C temperature rise. Coiltronics at (305) 781-8900, or Hurricane Labs at (801) 635-2003 can supply this inductor off the shelf.

Capacitors

Ripple current in the output capacitors C2 and C3 is 250mA$_{RMS}$ total with the input voltage at 30V and maximum load on the two outputs.

The input capacitor (C1), which undergoes higher stress, has a ripple current of 830mA maximum at 14V input and maximum load.

The input and output capacitors have been chosen primarily for ESR, not for voltage. The 50V rating of the capacitors is not due to stress from the circuit but from the fact that the lowest ESR for a particular can size occurs at 50V, in this series of capacitors, from this specific manufacturer.

The capacitors in the frequency compensation network should be at least X7R ceramic, never Z5U, and if broad temperature operation is expected, polyester or polycarbonate film caps should be used.

Circle No. 53

Layout

In order to achieve proper performance it is important to lay out the circuit as shown in Figure 1. Use a single point ground at the output of the converter as shown. The term "short" indicates that the trace should be as short as possible between the two points shown. These traces should have a minimum width of 0.2" in 2 oz. copper for a length of less than 1.5". Traces longer than this should be avoided on heavier lines of the schematic.

Heat Sinking

Any heat sink of 30°C/W or lower will keep the LT1076 at an acceptable temperature up to a 70°C ambient. See the LT1076 data sheet for further information.

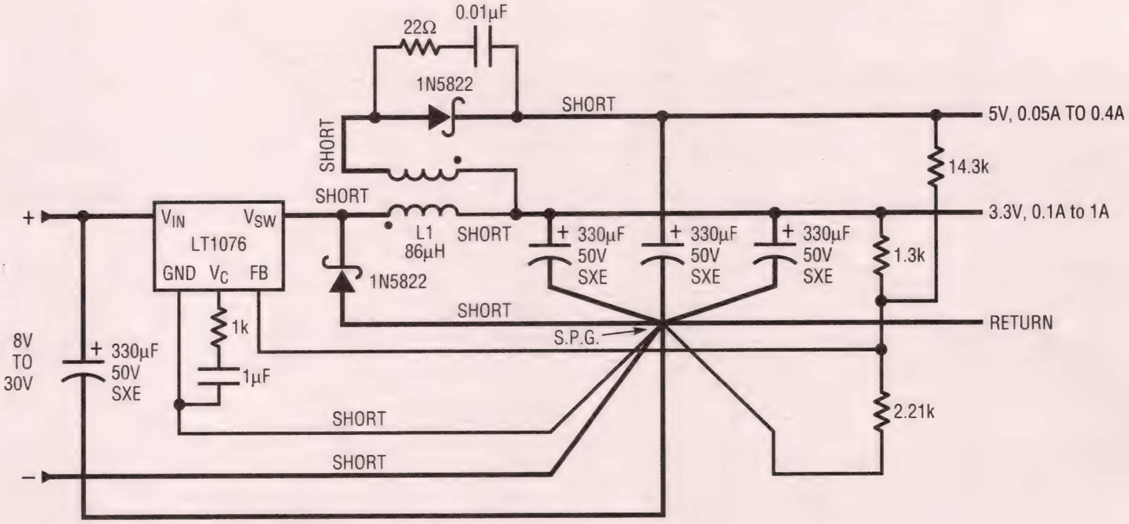

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Figure 1. 3.3V to 5V Dual Output DC/DC Converter

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JFET improves peak detector's accuracy

Mika Maaspuro, Jouko Kurki, Christer Holmlund, Kimmo Ahola, VTT Technical Research Centre of Finland, Espoo, Finland

The conventional diode-based peak detector just does not have enough accuracy for today's 12-bit, or greater, D/A converters. In **Fig 1**, the peak-detector circuit, JFET Q_1, acting as a voltage-controlled resistor, replaces the usual diode. The circuit controls Q_1, so that the voltage at the noninverting input of op amp IC_{1B} follows the *rising* edge of an input pulse. When the peak value of the input pulse passes, the circuit drives the gate voltage of Q_1 to negative saturation, locking the circuit's output at the input's peak voltage.

Q_1's gate bias must be at the JFET's pinch-off voltage when no input is present. Because the pinch-off voltage varies among individual JFETs, you must use R_1 to trim the circuit. Diode D_1 keeps the output of op amp IC_{1A} in the middle of its output range. Otherwise, IC_{1A} would be at its negative saturation voltage. D_1 is essential for maximizing the speed of the peak detector.

If your input pulse has sharp edges, damped oscillations may occur at these edges but should pose no problems. For semigaussian pulse shapes, the circuit's output is always stable after seeing a maximum input. You should optimize the values of capacitor C_1 and resistor R_2 to suit your input pulses' shapes.

The lag that op amp IC_{1A} introduces when driving its output to saturation can cause a small output error—especially for large input-pulse amplitudes. You can reduce this error slightly by decreasing the value of R_2.

The best choice for Q_1 is a fast RF FET such as the 2N4416. C_1 should be a polypropylene capacitor, such as the EVOX PMR series. The file DI1128Z.ZIP, posted on the EDN Reader's BBS, contains a longer writeup and test data. **EDN BBS /DI_SIG #1228**

To Vote For This Design, Circle No. 396

References

1. Graeme, J, "Feedback tames detector overshoot," *EDN*, April 25, 1991, pg 182.

2. Counts, L and M Murphy, "Peak detector circuit captures 200-ns pulses," Analog Dialogue 24-2, 1990, Analog Devices Inc, Norwood, MA.

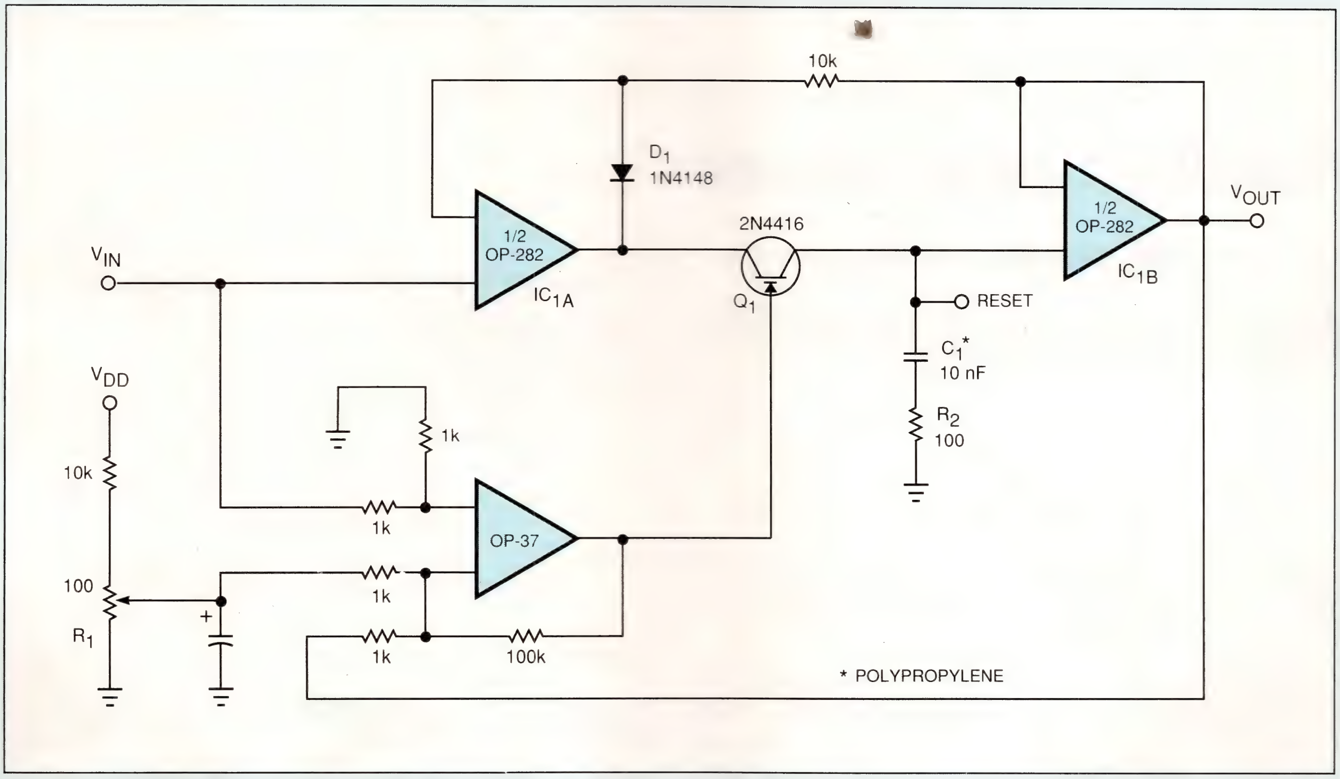

Fig 1—This high-accuracy peak detector's JFET outperforms the usual peak detector's diode.

Absolute-position sensor exhibits 1% linearity

David Barker, Teletrac, Goleta, CA

By aligning the sensitive axis of an analog Hall-effect device *perpendicular* to the axis of a magnet, you can obtain a highly linear position sensor. The technique works best with magnets having at least a 4:1 length to pole-face diameter ratio. Between their poles, such magnets' flux lines exit the magnet nearly normal to the magnets' axes. Long, thin magnets will evince monotonic outputs, but their signals will become nonlinear in their midsection because of reluctance and saturation effects in the magnetic material.

Mount the Hall-effect sensor as close as possible to the surface of the magnet. With runout minimized, the sensor's output will be linear to 1% as it moves over the length of the magnet.

Applying this concept to a magnetic rotor yields a simple sine/cosine resolver that requires no ac excitation and provides constant-amplitude signals down to zero velocity. **EDN BBS /DI_SIG #1229**

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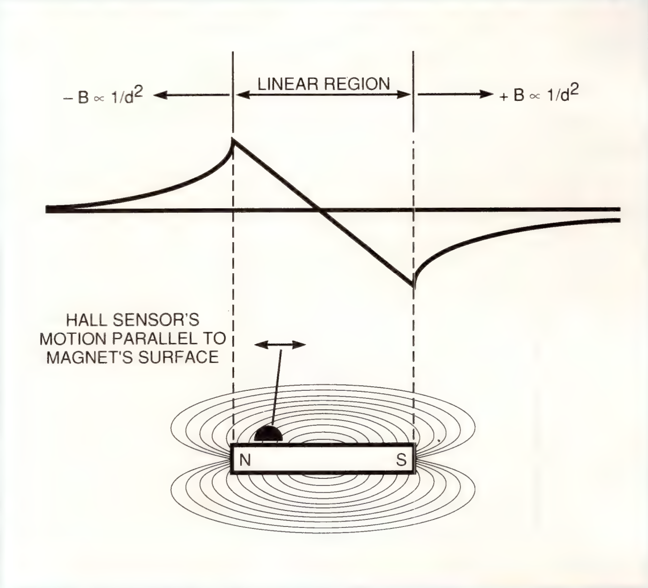

Fig 1—Mounting a Hall-effect sensor perpendicular to a magnet's axis yields a 1%-linear position sensor.

Algorithm exchanges elements

Kamran Husain, Mentor Programming Services Inc, Sugarland, TX

A program can exchange two elements without using a temporary variable using this algorithm

$$l \leftarrow l \oplus r$$
$$r \leftarrow r \oplus l$$
$$l \leftarrow l \oplus r$$

where "l" and "r" are the two elements being swapped. The algorithm will work for all bit sizes as long as the two items are both the same size.

You might want to use this technique not only because a processor's XOR instruction is usually faster than its MOVE instructions, but also because the algorithm saves stack space. Saving stack space is particularly advantageous in scientific-calculator programs.

Listing 1—Swap-algorithm example in C

```
#define EXCH(l,r)   (l) ^= (r); (r) ^= (l); (l) ^= (r);
#include "stdio.h"
int main(int argc, char *argv[]);

int main(int argc, char *argv[])
{
        int iA = 0xfeed; int iB = 0xcafe;
        long dA = 0xdead; int dB = 0xbeef;

        printf("\n...Using integers ");
        printf("\n Before exchange, A = %x, B = %x", iA, iB);
        EXCH(iA,iB)
        printf("\n After  exchange, A = %x, B = %x", iA, iB);

        printf("\n...Using long integers ");
        printf("\n Before exchange, A = %x, B = %x", dA, dB);
        EXCH(dA,dB)
        printf("\n After  exchange, A = %x, B = %x\n", dA, dB);
}
```

Listing 1 provides an example of the algorithm in C. **EDN BBS /DI_SIG #1231**

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CIRCLE NO. 100

Sensor adapts to changing light levels

Clive Bolton, Bolton Engineering Inc, Melrose, MA

The circuit in **Fig 1** dynamically adjusts itself, changing long-term conditions while monitoring the transparency of a medium. The circuit has two servo loops: one having a long time constant that maintains a steady level of light excitation through the monitored medium, and another having a short time constant that sets the threshold for detecting sudden changes in the medium's transparency.

The light-intensity servo loop drives LED D_1, keeping phototransistor Q_2's illumination constant over the long term. In operation, transconductance amplifier IC_{1C} converts the current output of phototransistor Q_2 to a voltage proportional to the light passing through the medium. Integrator IC_{1A} compares the light-level output against a fixed threshold set by R_1 and R_2. Voltage-to-current converter IC_{1B} and buffer Q_1 drive the LED D_1. IC_{1A}, R_3, R_4, and C_1 set this loop's time constant at ~66 sec.

Threshold comparator IC_{1D} reacts to sudden changes in light intensity. R_5 and C_2 have a time constant of 0.1 sec, filtering the incoming signal presented to IC_{1D}'s inverting input to prevent minor variations from causing a false alarm. R_6 and C_3, having a time constant of 10 sec, set the threshold at IC_{1D}'s noninverting input for detecting relatively sudden changes.

Resistors R_7 and R_8 reduce IC_{1D}'s threshold to ensure that the output will be inactive when the system is in steady state. R_9, D_2, and D_3 reduce the dark-to-light time constant of the threshold comparator to reduce the recovery time at the start of a cycle.

EDN BBS /DI_SIG #1230

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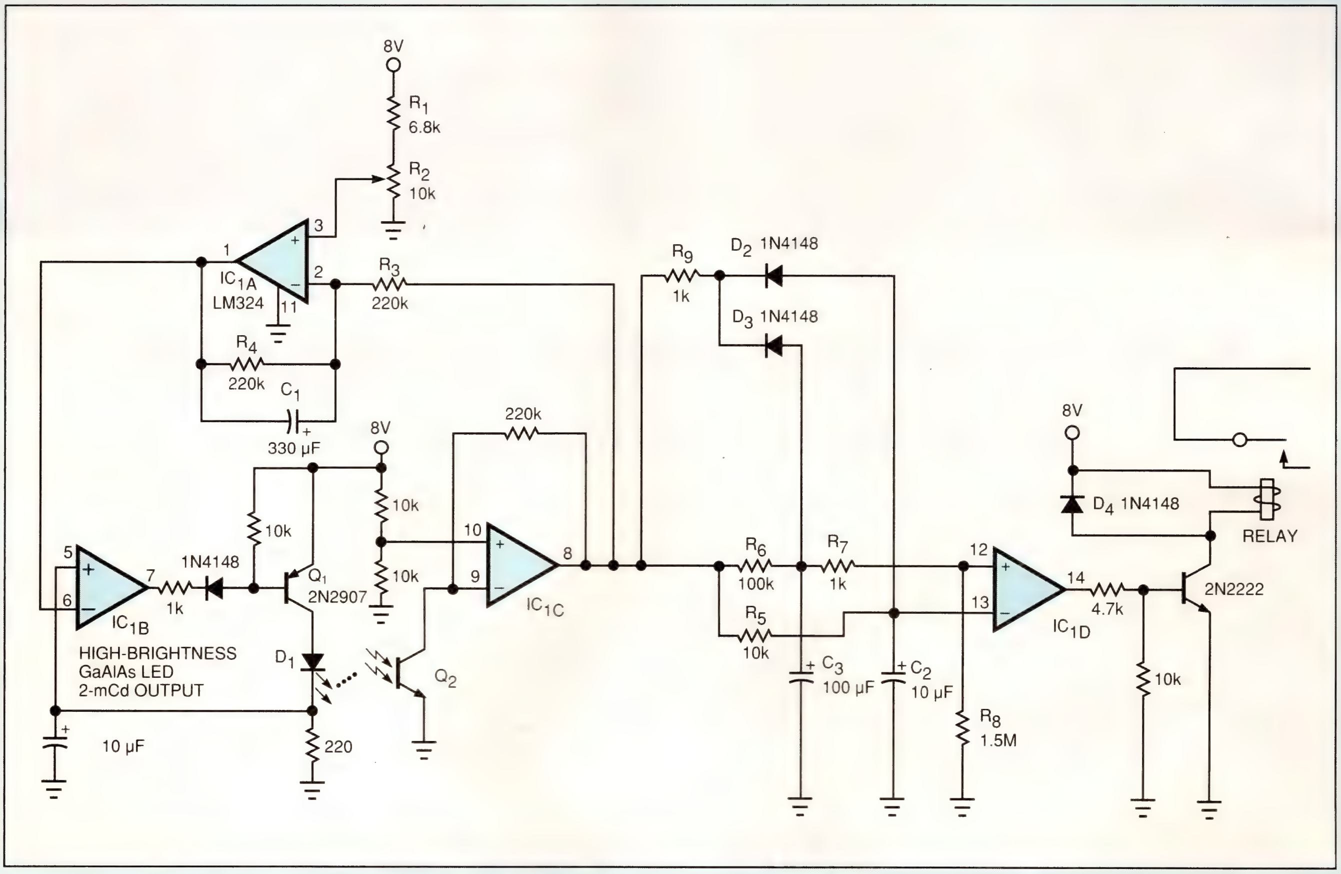

Fig 1—This circuit monitors a semitransparent medium, such as wastewater, placed between LED D_1 and phototransistor Q_2. The circuit adjusts to long-term changes in the medium, signaling only sudden changes.

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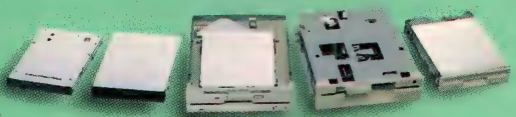

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CIRCLE NO. 101

FIFO tides over servo controller

Wes S Nakamura, Institute for Astronomy, Honolulu, HI

The circuit in **Fig 1** lets servo systems survive intense bursts of incremental-encoder feedback signals without losing count. This situation is especially prevalent in servo systems having high speed, high positional resolution, and high friction and "stiction."

The circuit's quadrature decoder accepts the encoder's (not shown) output at rates faster than a servocontroller (also not shown) can process. The circuit temporarily stores inputs in a FIFO memory, clocking them out to a servocontroller at a rate the servocontroller can accept. So, for example, an HCTL-1100 servocontroller, which normally cannot accept encoder pulse widths less than 1.6 μsec, can ride through momentary bursts having 375-nsec pulse widths.

Four state machines (**Fig 2**), burned into two PAL devices, control the circuit. An HCTL-2020 quadrature decoder, IC_5, clocked at 8 MHz accepts quadrature-signal pulse widths as narrow as 375 nsec from CHA_IN and CHB_IN. For every encoder count received, IC_5 outputs a clock pulse, CNT_CLK and up/down direction bit, UP_DOWN, at pins 16 and 5. The clock pulse, CNT_CLK, then sets flip-flop IC_3's ready signal, RDY. The clock pulse also latches the

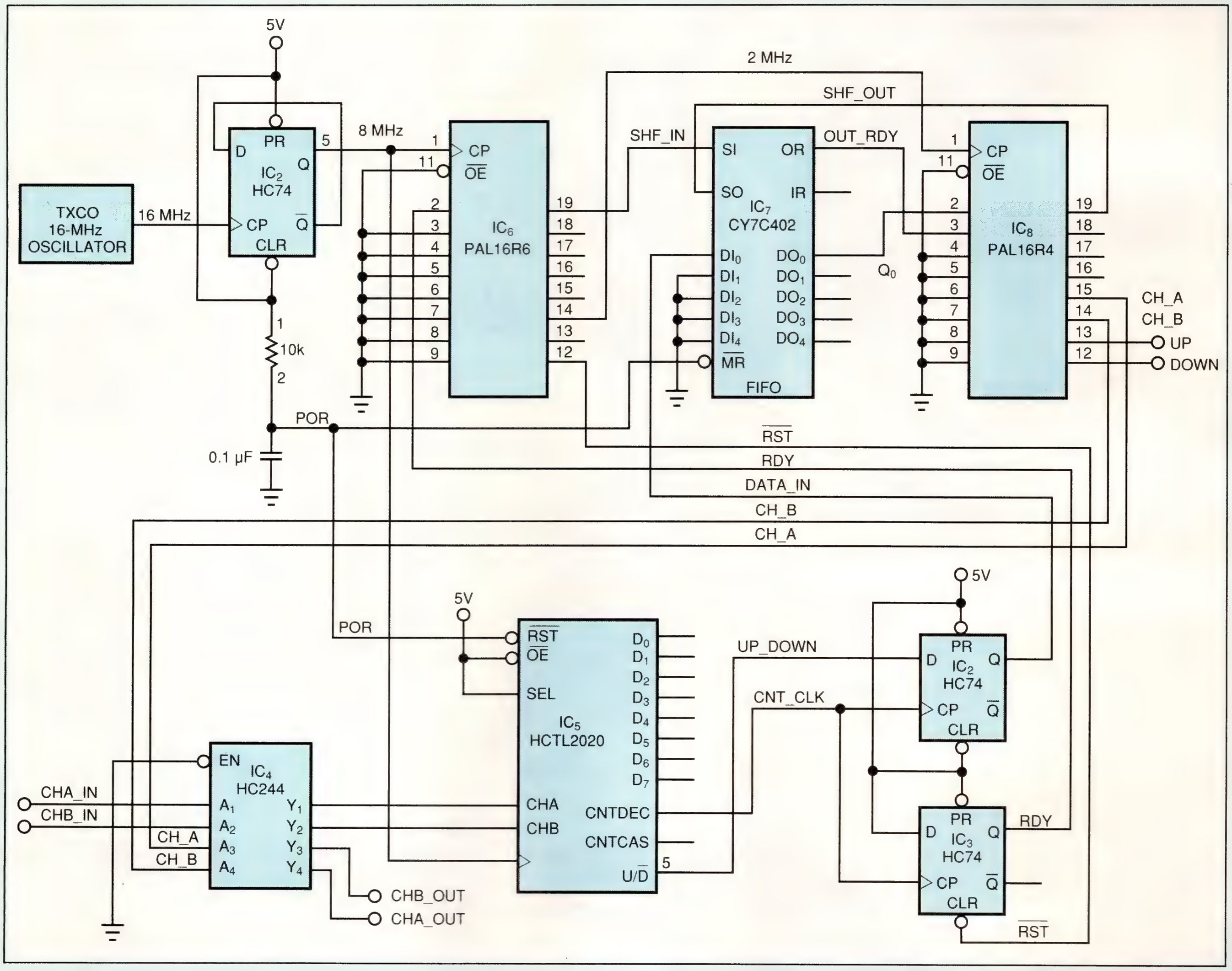

Fig 1—If a servo system's feedback pulses come in faster than the servo controller can handle them, this circuit temporarily stores the signals in a FIFO-memory IC, clocking them out later at the proper rate. Two PAL devices hold four state machines that control the circuit (Fig 2).

UP_DOWN direction-count signal into flip-flop IC$_2$. This latched signal, DATA_IN, is an input for a Cypress CY7C402 FIFO, IC$_7$.

State machine 1 in PAL16R6, IC$_6$, detects the new increment by polling the RDY signal. State Machine 1 then loads the logic value of DATA_IN into the FIFO, finally clearing the RDY output of IC$_3$ for the next decoder count.

When FIFO IC$_7$ has the up/down count loaded, OUT_RDY signal IC$_7$, pin 16 becomes asserted, indicating the new count is available at the FIFO's output. State machine 3, which resides in a PAL16R4, IC$_8$, unloads the FIFO and, depending on whether the count indicates up or down, increments or decrements State machine 4—also in IC$_8$. State machine 4 outputs the appropriate quadrature signals from pins 15 and 14 of IC$_8$. After buffering, these new quadrature outputs go the servo controller as CHA_OUT and CHB_OUT.

State machine 2—a simple frequency divider—in IC$_6$ clocks both state machines 3 and 4. They are, in this case, running slower than state machines 1 and 2 by a factor of 4. Thus the output is guaranteed to have pulse widths at least 2-msec wide. In effect, the outputs CHA_OUT and CHB_OUT simply follow the increment or decrement activity of CHA_IN and CHB_IN. When the pulse widths of CHA_IN and CHB_IN are narrower than 2 μsec, CHA_OUT and CHB_OUT effectively stretch the pulse widths to 2 μsec. The FIFO stores any ensuing backlog of encoder counts until dumping them out to the servocontroller becomes possible.

The EDN Reader's BBS contains CUPL **listings** and documentation for the two PAL devices in **Fig 1.** From the Main System Menu, enter ss/di_sig, then rk#1200.
EDN BBS /DI_SIG #1200

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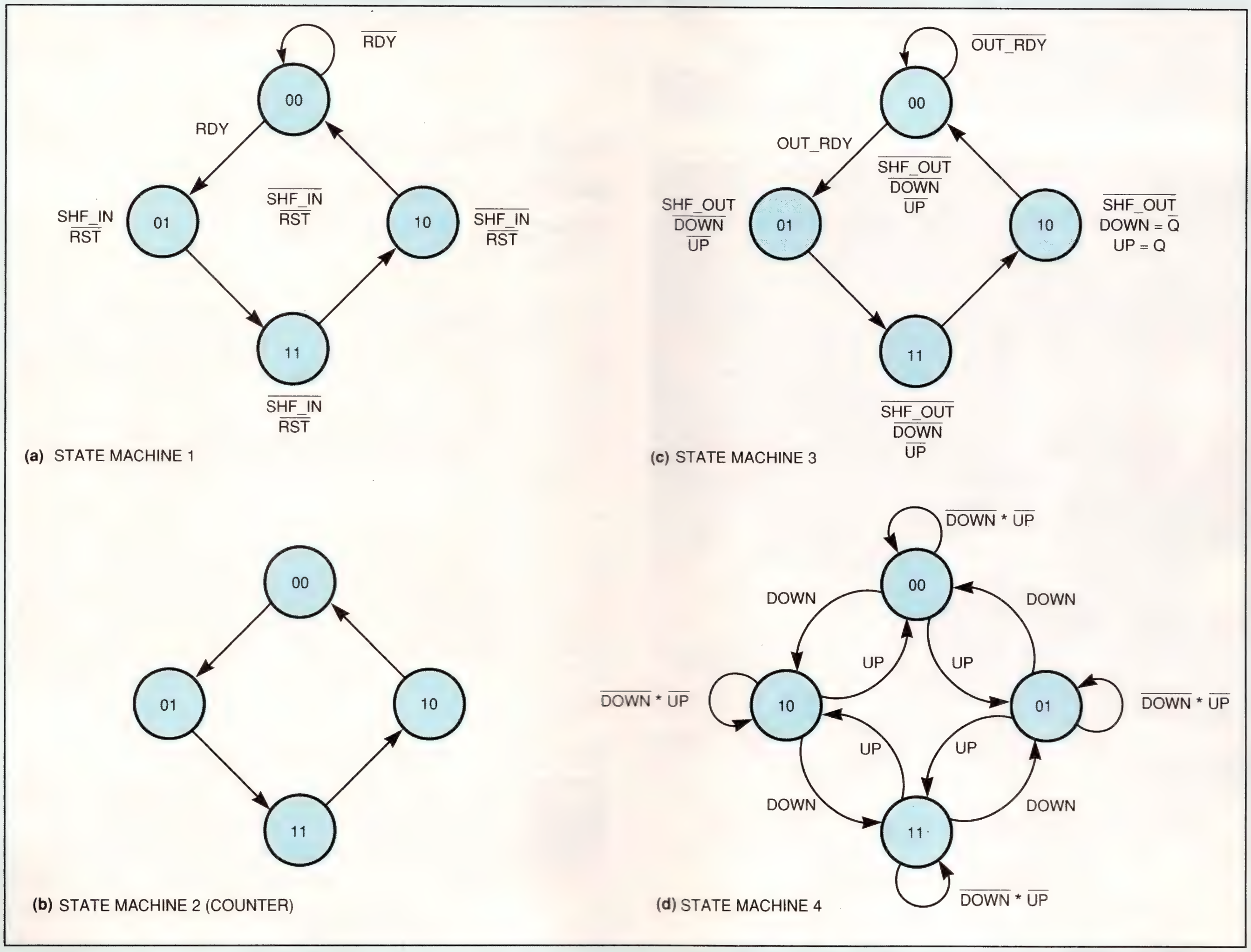


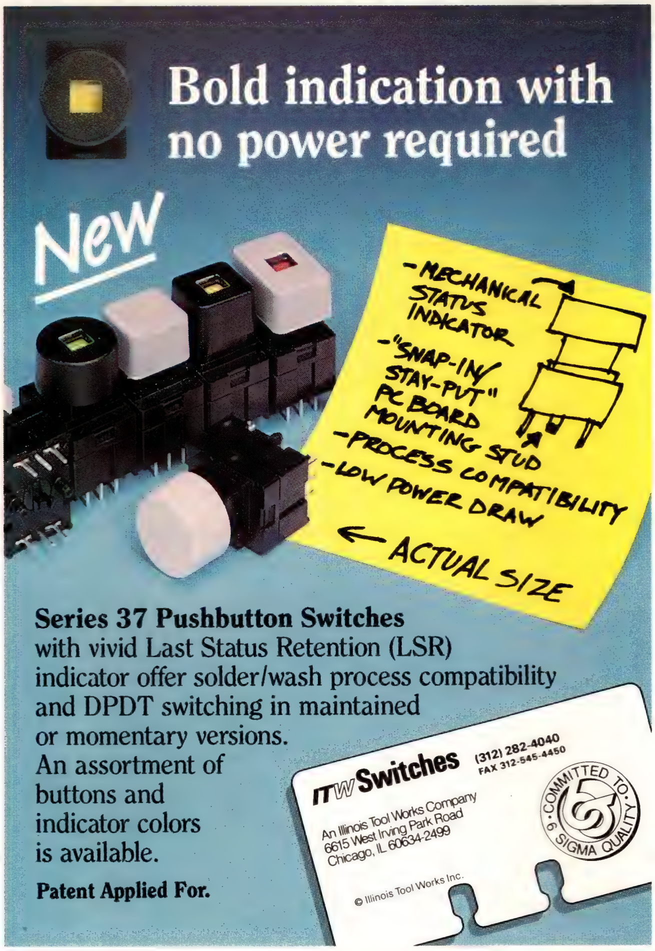
(a) STATE MACHINE 1

(c) STATE MACHINE 3

(b) STATE MACHINE 2 (COUNTER)

(d) STATE MACHINE 4

Fig 2—These four state machines control the circuit in Fig 1. State machine 1 (a) shifts data into the FIFO. State machine 2 (b) is a simple frequency divider. State machine 3 (c) shifts signals out of the FIFO by clocking state machine 4 (d) up or down.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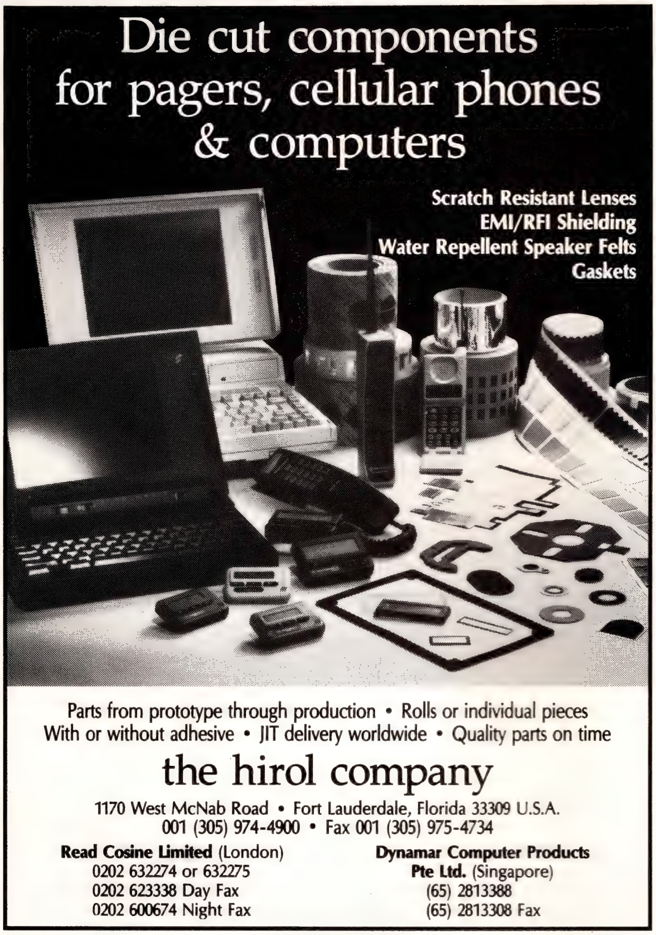
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CIRCLE NO. 103

Software Shorts

PLD snags highest number

Robert Micheletti, Printrak International Inc
Anaheim, CA

The suite of files in **EDN BBS /DI_SIG #1232** contains a circuit diagram and programming information for a 22V10-based, 8-bit magnitude comparator. Combined with a latch, the PLD retains the highest value it sees in a data stream.

To Vote For This Design, Circle No. 397

Spice simulates sawtooth generator

Charles Hymowitz, Intusoft
San Pedro, CA

The generator in the parametrized Spice **listing** in **EDN BBS /DI_SIG #1234** develops a sawtooth waveform.

To Vote For This Design, Circle No. 398

Single EPLD provides parallel to biphase encoding

William Grill, Riverhead Systems
Littleton, CO

The EPLD files in **EDN BBS /DI_SIG #1235** program an Intel 85C22V10-15 as a versatile parallel to a biphase encoder. The encoder selectively offers S, M, or L encoding formats.

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Read-channel chip set. The PCA3650 2-chip set for hard-disk drives accommodates zone bit recording (ZBR). It has AGC, a programmable filter, a pulse detector, and a quad peak-servo detector. The PCA3660 has a data separator, a frequency synthesizer, programming DACs for ZBR, and encoding and decoding 1.7 code. Both devices come in 44-pin plastic quad flatpacks. $15 (1000). **GEC Plessey Semiconductors,** 1500 Green Hills Rd, Scotts Valley, CA 95067. Phone (408) 439-6038.

Circle No. 501

Read-channel ICs. The CL-SH3300 and CL-SH4400 are synchronous read-channel ICs. The CL-SH3300 requires only two decoupling and two bypass capacitors. The chip handles digital data rates of 48 Mbps to and from the head assembly. The CL-SH4400 is the digital portion of a 2-chip read/write channel that provides data transfer rates as high as 64 Mbps. CL-SH3300, $25; CL-SH4400, $27 (1000). **Cirrus Logic Inc,** 3100 W Warren Ave, Fremont, CA 94538. Phone (510) 623-8300. FAX (510) 226-2240.

Circle No. 502

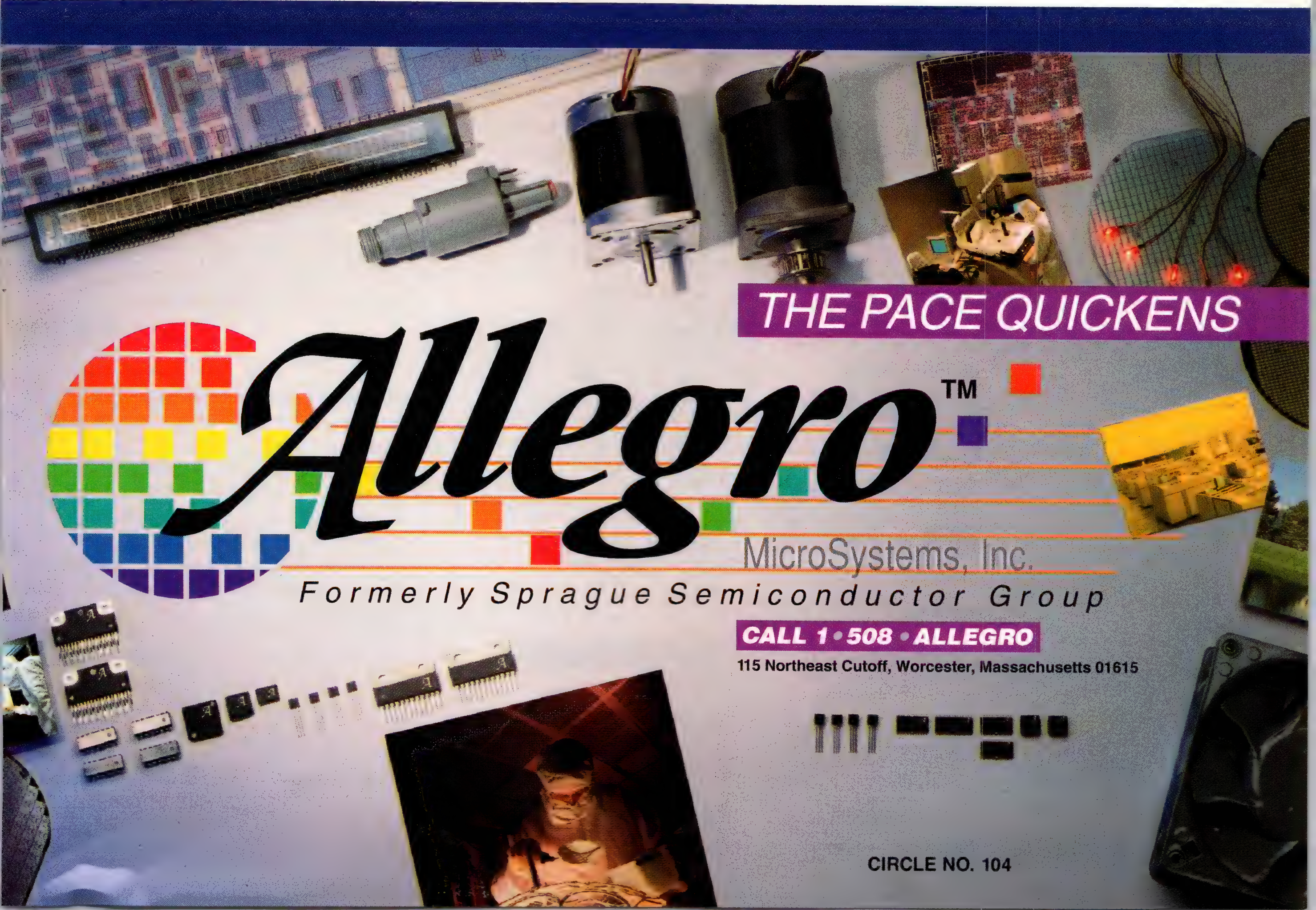
Laser-printer dot controller. The AD9560 PWM IC controls the dot duty cycle and pulse position in laser printers. It provides 256 levels of gray scale. To obtain high-resolution gray scale, the chip's PWM device sets the pulse driving the laser diode from 0 to 100% in 256 steps. You can also set the pulse position to the beginning, middle, or end of the dot clock period. $15 (1000). **Analog Devices Inc,** 7910 Triad Center Dr, Greensboro, NC 27409. Phone (919) 668-9511. FAX (919) 668-0101.

Circle No. 503

Mixed-voltage ISA bus controller. The WD8110 interfaces with the 486SX/DX family of µPs. The mixed-voltage IC handles clock speeds of 50 MHz at 5V and 33 MHz at 3.3V. Power-management features include a system-activity monitor, peripheral power control, CPU sleep and power-down, and suspend. The Immunizer virus-protection feature uses the System Management Interrupt and a proprietary antivirus circuit to protect all areas of the hard disk. $30 (1000). **Western Digital Corp,** 8105 Irvine Center Dr, Irvine, CA 92718. Phone (714) 932-6000.

Circle No. 504

Bus-interface register. The MC74F823 9-bit bus-interface register is a member of the company's Fast Schottky TTL logic family. The buffered register has noninverting outputs, which interface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CIRCLE NO. 104

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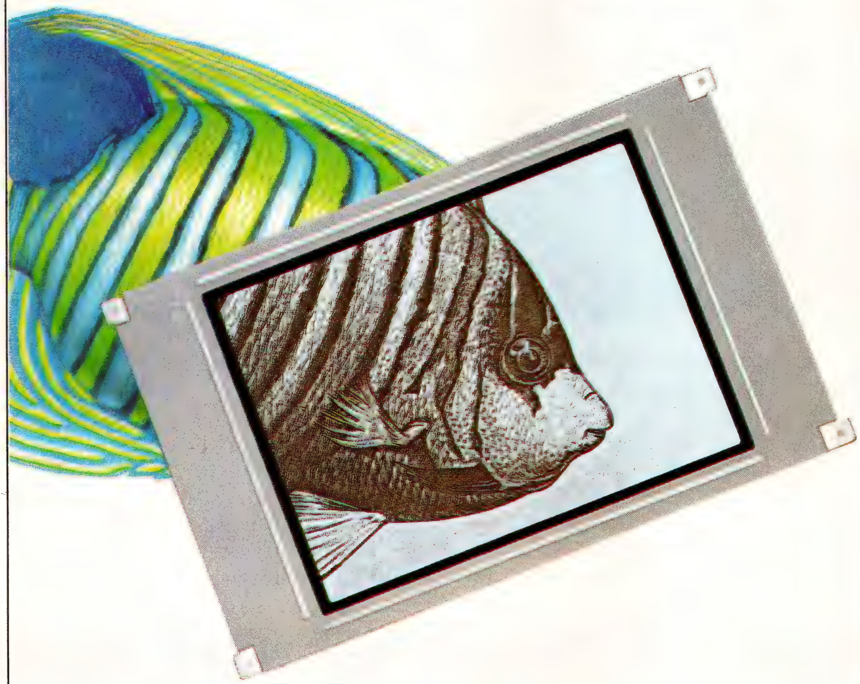

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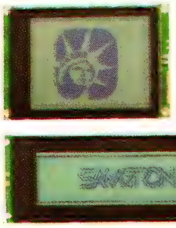

For Graphic Display Modules

Dots or Pixels (W x H)	Model No	Module Size (W x H)	Viewing Area (W x H)
640 x 480 (B/W)	UG-641-01	257 x 158.5 x 10.0	180.0 x 135.0
	UG-641-02	263.5 x 169 x 9.0	198.0 x 150.0
640 x 200	UG-64E-05	270 x 104 x 7.5	236.4 x 78.0
480 x 128	UG-48D-01	270 x 110 x 11.1	242.0 x 69.0
	UG-48D-02	268 x 94 x 11.5	231.5 x 66.0
480 x 64	UG-48B-01	296.8 x 78 x 11.7	239.4 x 38.1
	UG-48B-03	260 x 58 x 12.0	229.5 x 36.0
320 x 240	UG-32F-01	143 x 96.8 x 12.0	104.0 x 79.3
240 x 64	UG-24B-03	180 x 65 x 12.0	132.0 x 39.0
	UG-24B-04	149 x 57 x 12.0	117.0 x 41.0
128 x 64	UG-13B-01	93 x 70 x 8.5	70.7 x 38.8
	UG-13B-02	113 x 65 x 11.5	73.4 x 38.8

* The above spec. may be changed by Rev. No.

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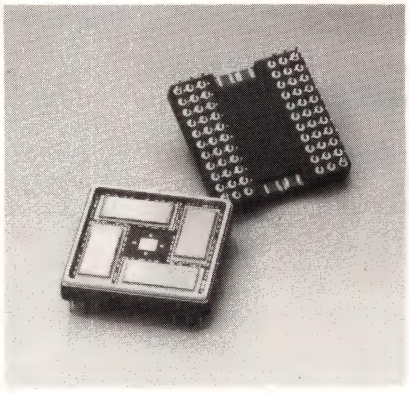
Head Office 12th Fl., Daekyung Bldg., 120, 2-Ka Taepyung-Ro, Chung-Ku, Seoul 100-102 Korea Tel: (2) 727-3351/3 Fax: (2) 756-9111 **Samtron Display Inc. (SDI)** 14251, East Firestone Blvd., Suite 101 LA Mirada CA 90638 USA Tel: (310) 802-8425 Fax: (310) 802-8820 **Samtron Frankfurt Office** Tel: 06196-483829/3 Fax: 06196-483321 **Tokyo Office** Tel: (813) 3258-8550 Fax: (813) 3258-8534 **Hong Kong Office** Tel: (852) 862-6053 Fax: (852) 866-1242 **London Office** Tel: (4481) 862-9311/2 Fax: (4481) 862-0096/7 **Singapore Office** Tel: (65) 534-5301 Fax: (65) 534-3429

CIRCLE NO. 105

with buses having parity. The register consists of nine D-type, edge-triggered flip-flops having 3-state outputs. Buffered-clock and output-enable lines are common to all flip-flops. The chip also has an asynchronous clear line. $2.07 (100). Delivery, seven to nine weeks ARO. **Motorola Inc,** MD M544, 2200 W Broadway, Mesa, AZ 85202. Phone (602) 962-2085. FAX (602) 898-5020.

Circle No. 505



4-Mbit SRAM. The EDI8C32128C static RAM contains four 128k × 8-bit dice in a multidie-in-cavity ceramic pin-grid-array. The package fits 4 Mbits of memory into 1.3 in.^{2} of board space. Available access speeds are 25, 35, 45, and 55 nsec. The module has separate chip enable and write enable controls for each 128k × 8-bit section, which allows access as a ×8, ×16, ×24, or ×32-bit-wide device. The 25-nsec version, $725; 55-nsec version, $580 (100). Delivery, 12 weeks ARO. **Electronic Designs Inc,** 1 Research Dr, Westborough, MA 01581. Phone (508) 366-5151. FAX (508) 836-4850.

Circle No. 506

PLL frequency synthesizer IC. The HD155001T contains a 1.1-GHz prescaler and operates from 2.7 to 5V. The dual modulus pulse-swallowing synthesizer has a selectable 64/65 or 128/129 divide ratio and a lock detector. Designed for analog cellular phones, the system's μC places the chip in a power-savings mode during standby. The power-savings mode turns off the prescaler, disables the clock, and places the chip's charge pump in a high-impedance state. $5.15 (1000). **Hitachi America Ltd,** Semiconductor & IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 285-1601, ext 06; (415) 589-8300. FAX (415) 583-4207.

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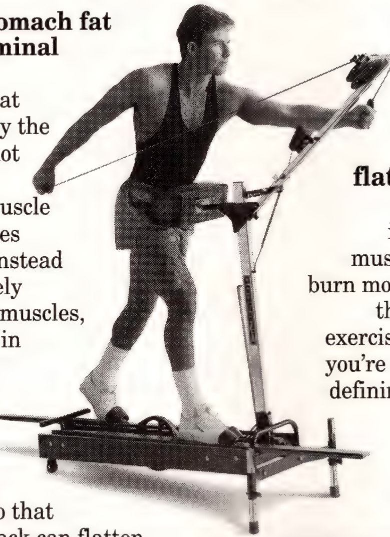

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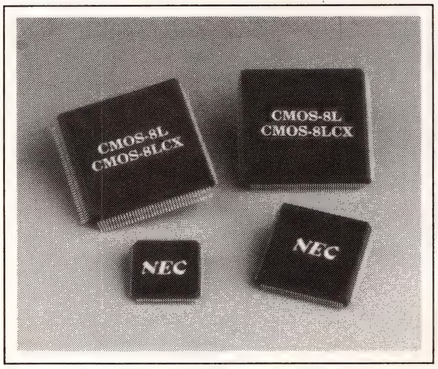
CIRCLE NO. 24

IEEE-488.2 controller chip. The NAT4882 controller chip for the IEEE-488.2 bus is register compatible with NEC's μPD7210 and TI's TMS9914A microcontroller chips. It controls and monitors all of the bus handshake lines and has a timer, which can set bus time-out values. The chip runs at a clock rate of 20 MHz and does not transmit data or commands when there is no listener. It also performs service requests. $25. **National Instruments,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 508**



3.3V gate arrays. The CMOS-8L is a 3.3V gate-array family fabricated in a 0.5-μm process. The family offers gate densities ranging from 11,000 to 627,000 gates and a gate delay of 131 psec for a 2-input NAND gate driving one load. The current implementation can handle interface data rates as fast as 75 MHz. Average power dissipation per gate is 1.25 μW/MHz. A proprietary 5V interface allows the chip to communicate with 5V devices without damage to the chip. $6 to $50. **NEC Electronics Inc,** Box 7241, Mountain View, CA 94039. Phone (415) 965-6000. FAX (415) 965-6130. **Circle No. 509**

32-bit RISC μP. The V_R3800 is a derivative of the Mips V_R3000 RISC (reduced-instruction-set-computer) μP. The chip is designed for embedded-control applications and delivers 30 VAX MIPS when operating at 25 MHz. The 0.8-μm CMOS chip operates from 5V and consumes 2W when operating at 25 MHz. The chip comes in 16-, 20-, and 25-MHz versions and integrates the CPU core, a 4-kbyte instruction cache, a 1-kbyte data cache, a bus interface, and a PLL clock generator. 25-MHz version, $49 (1000). **NEC Electronics Inc,** Box 7241, Mountain View, CA 94039. Phone (415) 965-6000. **Circle No. 510**

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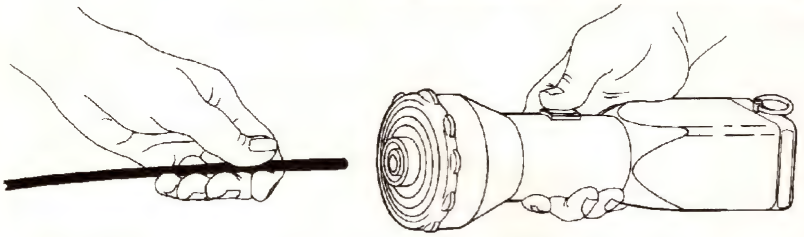

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Voltage references. The REF1004-1.2 and REF1004-2.5 are 2-terminal 1.2 and 2.5V bandgap voltage-reference diodes, respectively. The 1.2V device operates over a 10-µA to 20-mA current range, and the 2.5V device operates over a 20-µA to 20-mA current range. Active laser trimming provides tight voltage tolerances. The devices operate over the extended temperature range of -40 to +85°C. The chips come in an 8-pin SOIC. $1.55 (1000). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. **Circle No. 511**

Board test driver. The Bt694 pin-diode driver is designed for pc-board automatic test equipment. The chip features 750 mA of output current and an output impedance of less than 1Ω. You can adjust the output slew rate from 0.025-to 1V/nsec. The inputs to the chip are differential and compatible with ECL, TTL, and CMOS logic families. The chip also has a thermal monitoring circuit. $49 (100); evaluation module, $99. **Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 535-3510. FAX (619) 452-1249. **Circle No. 512**

Video RAMDAC. The Bt885 CacheDAC has a dedicated video port that lets you mix graphics and video data to display a full-motion video window in a desktop system. The chip can asynchronously load video data and a graphics pixel stream while maintaining a 135-MHz throughput for 1280×1024-pixel displays. The chip accommodates 32-bit graphics and 32-bit pixel ports and is compatible with both video-RAM and dynamic-RAM video systems. $42.65 (100). **Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. FAX (619) 452-1249. **Circle No. 513**

4-bit µCs. Three additions to the company's 75X family of 4-bit CMOS microcontrollers operate as low as 2V. The µPD75308B series has an LCD controller and drives 128 segment displays. Three versions of the chip have 4-, 6-, or 8-kbytes of ROM and 512×4-bits of RAM. When operating at 4.19 MHz, they have an instruction cycle time of 0.95 µsec. $3.90 to $4.20 (10,000); emulation system, approximately $7800. **NEC Electronics Inc,** Box 7241, Mountain View, CA 94039. Phone (415) 965-6000. FAX (415) 965-6130. **Circle No. 514**

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Divide-by-four prescalers. The IFD-53110 and IFD-53010 divide-by-four frequency dividers operate as high as 3.5 and 5.5 GHz, respectively. The silicon bipolar MMICs (monolithic microwave ICs) come in 4-lead, 100-mil hermetic metal ceramic surface-mount packages with gold-plated leads. The ECL-compatible dividers have a phase noise of -143 dBc/Hz at 1 kHz. IFD-53010, $76; IFD-53110, $37.50. **Hewlett-Packard Co,** Box 58059, Santa Clara, CA 95052. Phone (800) 227-1817. **Circle No. 516**

Radio-data-system demodulator. The SAA6579 Radio Data System (RDS) demodulator features on-chip antialiasing, bandpass, and signal-reconstruction filters. The chip requires only six passive components and a crystal to recover RDS data from FM radio broadcasts. The RDS data provides information on network/station names, date, time, and traffic conditions. The chip provides the data and a clock output. A Costas loop demodulator uses an external 4.332- or 8.664-MHz crystal. US$2.20 (OEM qty). **Philips Semiconductors,** Box 218, Building BAF-1, 5600 MD, Eindhoven, The Netherlands. Phone +31 40 722091. FAX +31 40 724825. **Circle No. 517**

Variable gain-control amplifiers. The IVA-14228 and IVA-14208 are silicon bipolar MMIC (monolithic microwave IC) variable-gain amplifiers. They operate as high as 2.5 GHz and can transmit digital data at 3.4 Gbps/sec. Both input and output levels can be single-ended or differential. Typical gain is 24 dB, and the control range is 34 dB. Gain control response is 10 nsec typically. IVA-14208 in plastic SO-8 package, $9.95; IVA-14228 in hermetic metal/ceramic package, $54.50. **Hewlett-Packard.** Box 58059, Santa Clara, CA 95052. Phone (800) 227-1817.
Circle No. 518

4-Mbit DRAMs. The HM51S4900A/AL and HM51S4280A/AL 4-Mbit dynamic RAMs (DRAMs) have 512k × 9-bit and 256k × 18-bit parity organizations, respectively. Versions are available with maximum access times of 70, 80, or 100 nsec. The DRAMs feature a self-refresh mode, which reduces power by extending the refresh interval from the standard 15.6 to 125 μsec. When the RAS line remains low for 100 μsec, the DRAM automatically initiates the self-refresh mode. HM51S4900AJ-8 80-nsec version, $28.70 (100). **Hitachi America Ltd,** Semiconductor & IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 285-1601, ext 11; (415) 589-8300. **Circle No. 519**

Battery-charge controllers. The MAX712 and MAX713 each contain an ADC, analog power-control circuitry, and intelligence to fast- and trickle-charge NiCd and NiMH batteries. The devices charge from 1 to 16 cells connected in series and automatically switch from fast- to trickle-charge to prevent overcharging. The ICs use voltage-slope, temperature, and time-out detection to terminate charging. $3.09 (1000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 520**

14-bit multiplexer. The MX-826/883 14-bit analog multiplexer meets the MIL-STD-833 standard. It features a switching and settling time of 400 nsec max at 14-bit accuracy. Settling times to 12- and 10-bit accuracies are 225 nsec and 150 nsec max, respectively. The 8-channel device dissipates 575W max and comes in a 24-pin double DIP. $174. **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. **Circle No. 521**

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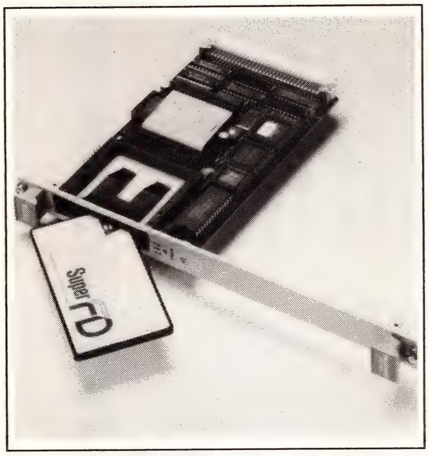


Contactless-memory-card interface. The CC155 VMEbus module reads and writes contactless memory cards. Inductive coupling between read/write circuits and an inserted card serves as the data-transmission medium. An 8051 processor in the module controls the transmissions. The module is available in 3HU and 6HU front-panel configurations. $1125. **Compcontrol Inc,** 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95032. Phone (408) 356-3817. FAX (408) 356-1755. **Circle No. 445**

SRAM PCMCIA cards. New static-RAM (SRAM) cards with capacities from 0.5 to 2 Mbytes comply with the PCMCIA (Personal Computer Memory Card International Association) 2.0 standard. All except the 2-Mbyte version are available with an automatically recharged auxiliary battery that backs up data when the main battery is being changed. The cards have 250-nsec read times and 150-nsec write times. They operate from a 5V supply, drawing 200 mA of current when accessed and 2 mA in standby mode. 1-Mbyte version with auxiliary battery, $186 (100). **Hitachi America Ltd,** Semiconductor & IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 285-1601, ext 16; (415) 589-8300. FAX (415) 589-4207. **Circle No. 446**

Floptical-disk drives. Floptical-disk drives for SCSI and parallel ports store 21 Mbytes of data on special 3½-in. floppy disks, which cost about $20 each. Two drives are for SCSI ports; one goes inside a computer, and the other attaches externally. A third drive attaches to a standard parallel port. Speed is roughly 3× that of conventional floppy-disk drives. $359 to $499. **Iomega Corp,** 1821 W 4000 S, Roy, UT 84067. Phone (800) 777-6179. **Circle No. 447**

PC/104 computer. The WCPU/104 80C88-based PC/104 computer module has 256 or 640 kbytes of onboard memory, standard BIOS, a speaker port, a keyboard port, and a reset connector. Signals of the industry-standard PC bus are available through the 64-pin PC/104 connector. $99. **Megatel Computer Corp,** 125 Wendell Ave, Weston, Ontario, M9N 3K9 Canada. Phone (416) 245-2953. FAX (416) 245-6505. **Circle No. 448**

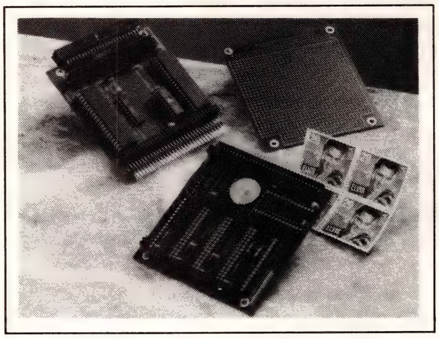
VME computer board. The XPX embedded PC is compatible with both the VMEbus and the PC/AT. An expansion architecture allows use of plug-on µP modules that can include the 80386DX, 80486DX, or 80486DX2 running at speeds from 20 to 66 MHz. The board is available with either 4 or 16 Mbytes of dynamic RAM. $2663 (100). **Logical Design Group Inc,** 6301 Chapel Hill Rd, Raleigh, NC 27607. Phone (919) 851-1101. FAX (919) 851-2844. **Circle No. 449**

VME X-Server. Vgs, an X-Server on a 6U VME board, performs fast graphics operations with an LSI Logic 33020 processor and a floating-point coprocessor. The 33020 combines a Mips R3000-compatible processor with hardware-assisted graphics functions such as bitblt and clipping. The unit's Xstone rating is greater than 60,000. $3500. **Vigra Inc,** 6044A Cornerstone Court, San Diego, CA 92121. Phone (619) 597-7080. FAX (619) 597-7094. **Circle No. 450**

VME64 computer board. The HK68/V4D, a 68040-based VME64 CPU board, has a 64-bit, 60-Mbyte/sec VME64 master-slave bus interface and on-card Ethernet and SCSI interfaces. The board comes with either 8 or 16 Mbytes of 2-way interleaved, dual-access dynamic RAM, up to 1 Mbyte of EPROM, 4 Mbytes of flash memory, and 512 bytes of nonvolatile RAM. A 200-Mbyte/sec Corebus mezzanine module with a PCMCIA (Personal Computer Memory Card International Association) 2.0 interface is an option. From $4995. **Heurikon Corp,** 8310 Excelsior Dr, Madison, WI 53717. Phone (800) 356-9602; (608) 831-0900. FAX (608) 831-4249. **Circle No. 451**

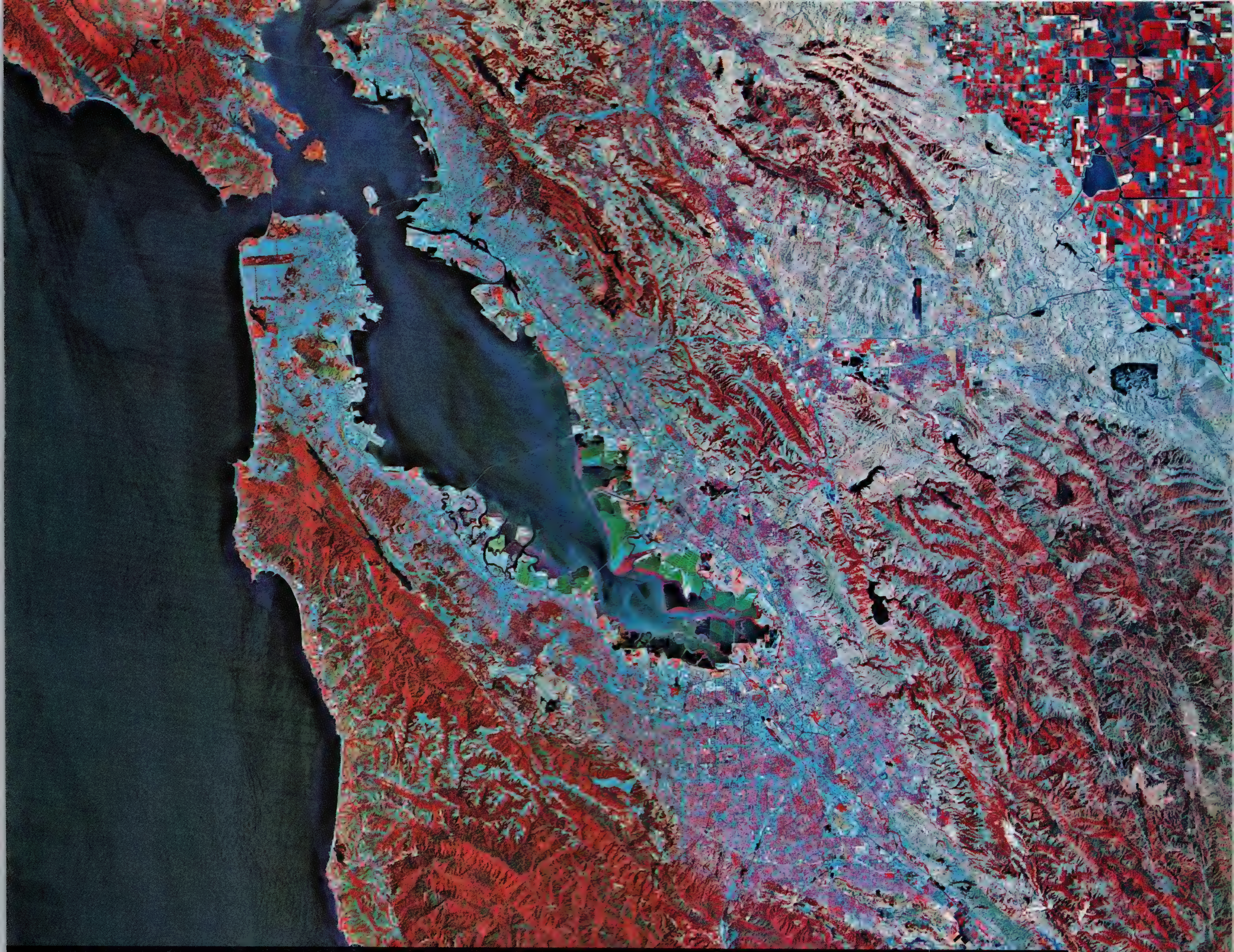
VME board for Ada. The commercially rugged MR-CPU330 runs Ada, but costs less than a MIL-STD board. With VADSworks, an Ada package from Verdix Corp, it can serve as a distributed host/target Ada development environment with TCP/IP and NFS support. The board was designed for extended operation at temperatures from -40 to +85°C; it has been tested against severe shock and vibration standards. From $5150. **Matrix Corp,** 1203 New Hope Rd, Raleigh, NC 27610. Phone (800) 848-2330. FAX (919) 231-8001. **Circle No. 452**

XGA-2 graphics card. The XGA-2 color graphics card works in ISA/EISA PCs and provides accelerated performance for OS/2 2.1 via IBM's XGA-2 graphics coprocessor. It also accelerates DOS applications running in VGA mode. Maximum resolution is 1360×1024. $499. **Radius Inc,** 1710 Fortune Dr, San Jose, CA 95131. Phone (408) 434-1010. **Circle No. 453**



PC/104 solid-state disk. The PCM-SSD is a PC/104 solid-state disk drive with sockets for as much as 2 Mbytes of RAM, EPROM, or flash memory. Designers can substitute their choices of semiconductor devices. The module measures 3.6×3.8 in., approximately the size of a 3½-in. disk. It stacks with other PC/104 modules. $195. **Winsystems,** 715 Stadium Dr, Suite 100, Arlington, TX 76011. Phone (817) 274-7553. FAX (817) 548-1358. **Circle No. 454**

FDDI for VME64. The PT-VME600 FDDI (Fiber Distributed Data Interface) node adapter for VME64 uses a 25-MHz Mips LR3300 RISC (reduced-instruction-set-computer) µP with an 8-kbyte instruction cache and a 1-kbyte data cache. It uses XLNT SMT station-management software and comes with a device-driver package for Unix System V. Two custom ASICs support the VMEbus interface. $3996 (100). **Performance Technologies Inc,** 315 Science Pkwy, Rochester, NY 14620. Phone (716) 256-0200. FAX (716) 256-0791. **Circle No. 455**



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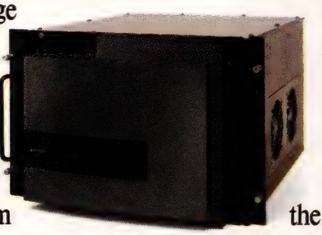

The DCRsi is the only data recorder that supports data rates from 0 to 240 Mbits/second and beyond in continuous, burst, or variable modes. This instantaneous response to the requirements of your application is what sets the DCRsi family apart from ordinary fixed-rate recorders.

The DCRsi can function like a true computer peripheral, making data reduction fast and efficient. And your job can be simplified even further with our line of off-the-shelf standard computer interfaces.

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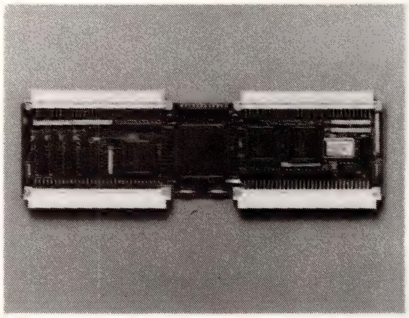
CIRCLE NO. 111

Military VME64 computer board. The CPU-40D VME64 computer board comes in five durability grades: conduction- and air-cooled Mil spec, conduction- and air-cooled rugged, and commercial. It has a 68040 μP and an expansion bus and can accommodate as much as 64 Mbytes of onboard dynamic RAM with byte parity. All the board's resources are on an internal bus, allowing extremely fast interactions between the processor and the VMEbus. From $8995. Delivery, six to eight weeks ARO. **Radstone Technology Corp,** 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; (201) 391-2700. FAX (201) 391-2899. **Circle No. 456**

VME memory module. The XVME-103 memory module provides as much as 8 Mbytes of EPROM or 4 Mbytes of flash memory. The 3U VMEbus module organizes memory into two independently addressable banks of four 32-pin sockets. Power-down memory protection ensures data integrity when using CMOS devices. $450 without memory. **Xycom Inc,** 750 N Maple Rd, Saline, MI 48176. Phone (800) 289-9266; (313) 429-4971. FAX (313) 429-3543. **Circle No. 457**



VME-to-Multibus II adapter. The LBXVME board allows a 6U VME board to install in a Multibus II chassis. The Multibus host processor transfers information to and from the LBXVME board, which then communicates with the attached VME device. The seven VME interrupts are mapped into the one LBX interrupt. $2305. **Applied Data Sciences Inc,** Box 814209, Dallas, TX 75381. Phone (214) 243-0113. FAX (214) 243-0217. **Circle No. 458**

Super VGA graphics card. WindowsVGA 24 is a 24-bit graphics accelerator for the ISA bus or the 32-bit VESA local bus. Model 8500 is for ISA; model 8500VL is for the local bus. Maximum resolution is 1280×1024; refresh rate is 72 Hz at 800×600 and 70 Hz noninterlaced at 1024×768. Model 8500, $179; model 8500VL, $199. **Genoa Systems,** 75 E Trimble Rd, San Jose, CA 95131. Phone (800) 934-3662; (408) 432-9090. FAX (408) 434-0997. **Circle No. 459**

STD32 Super VGA adapter. The zVID1 local-bus video adapter operates at the full speed of the system CPU, not at the slower speed of the bus backplane or of an ISA chip set. Video-select circuitry allows as many as seven processor cards, with video modules attached, to share a common display and keyboard. Each processor card can also have a separate video display. $595. **Ziatech Corp,** 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088. **Circle No. 460**

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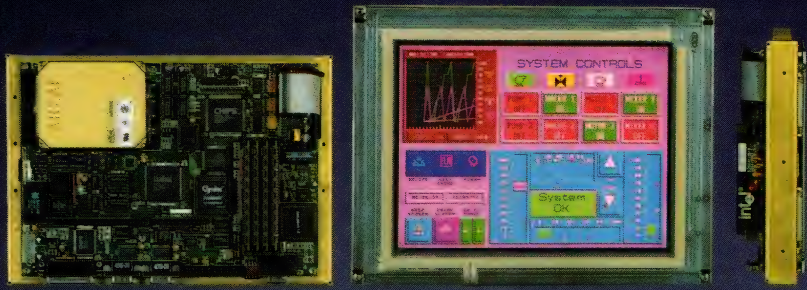

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CIRCLE NO. 112

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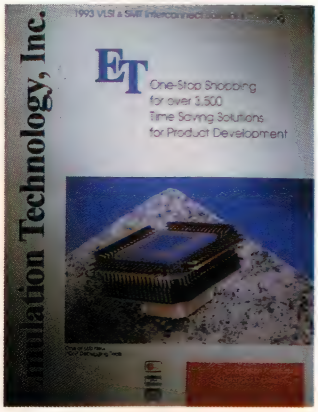
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CIRCLE NO. 113

VMEbus FDDI controller. The VCOM-47 Dual-Attach Single MAC Fiber Distributed-Data Interface (FDDI) controller interfaces VMEbus systems to X3T9.5 FDDI LANs. The controller's 25-MHz 68EC040 processor frees the host system from handling FDDI communications tasks. Separate 32-bit local buses—for the MC68839 FDDI System Interface; for 4 Mbytes of dynamic RAM; and for the CPU with 1 Mbyte of static RAM, 1 Mbyte of flash memory, and a peripheral-controller chip—further enhance performance. $4995 (100). **SBE Inc,** 2400 Bisso Lane, Concord, CA 94520. Phone (800) 925-2666; (510) 680-7722. FAX (510) 680-1427.

Circle No. 461

Macintosh LAN modem. The Optima 144 LAN modem for Macintosh computers comes with Hayesconnect 3.1A software, plus Appletalk remote-access software, Smartcom II Macintosh communications software, and cables. The modem transfers data at 14,400 bps; it also allows CCITT V.42 error control and CCITT V.42bis data compression for 57,600-bps data throughput. $549. **Hayes Microcomputer Products Inc,** Box 105203, Atlanta, GA 30348. Phone (404) 441-1617. FAX (404) 441-1213.

Circle No. 462

Super VGA touch monitor. The Truepoint TM-2 touch monitor combines a 14-in. Super VGA (1024×768) display, a high-resolution capacitive touch screen, controller, and mouse-emulation drivers for DOS, Windows, and OS/2. The 1024×1024 touch screen gives pixel-by-pixel control when touching the screen. The monitor works with all PCs, PS/2s, and compatibles. $1599. **MicroTouch Systems Inc,** 55 Jonspin Rd, Wilmington, MA 01887. Phone (508) 694-9900. FAX (508) 694-9980.

Circle No 463

Multiprocessor board. The FT860/2-V for VMEbus incorporates one or two Intel i860XP processors in a symmetrical, shared-memory architecture. Operating at 50 MHz, two processors combine to perform at 200 Mflops in a single 6U slot. The VME interface runs full bus mastership, allowing the board to operate as an independent single-board VME computer. $9000 to $14,000. **Alacron,** 71 Spitbrook Rd, Suite 204, Nashua, NH 03060. Phone (603) 891-2750. FAX (603) 891-2745.

Circle No. 464

STD 32 servo controller. The Model 4323 servo motor controller works in both STD 32 and STD 80 backplanes. Independent 32-bit DSP chips enable control of either one or two servo axes. Software drivers, compatible with the Ziatech Corp device-driver format, are linkable with Microsoft C, Turbo Pascal, Quick Basic, and assembly language. The 1-axis controller, $465; the 2-axis controller, $645. **Technology 80 Inc,** 658 Mendelssohn Ave N, Minneapolis, MN 55427. Phone (612) 542-9545.

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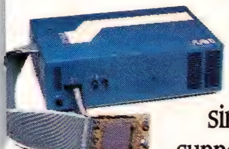

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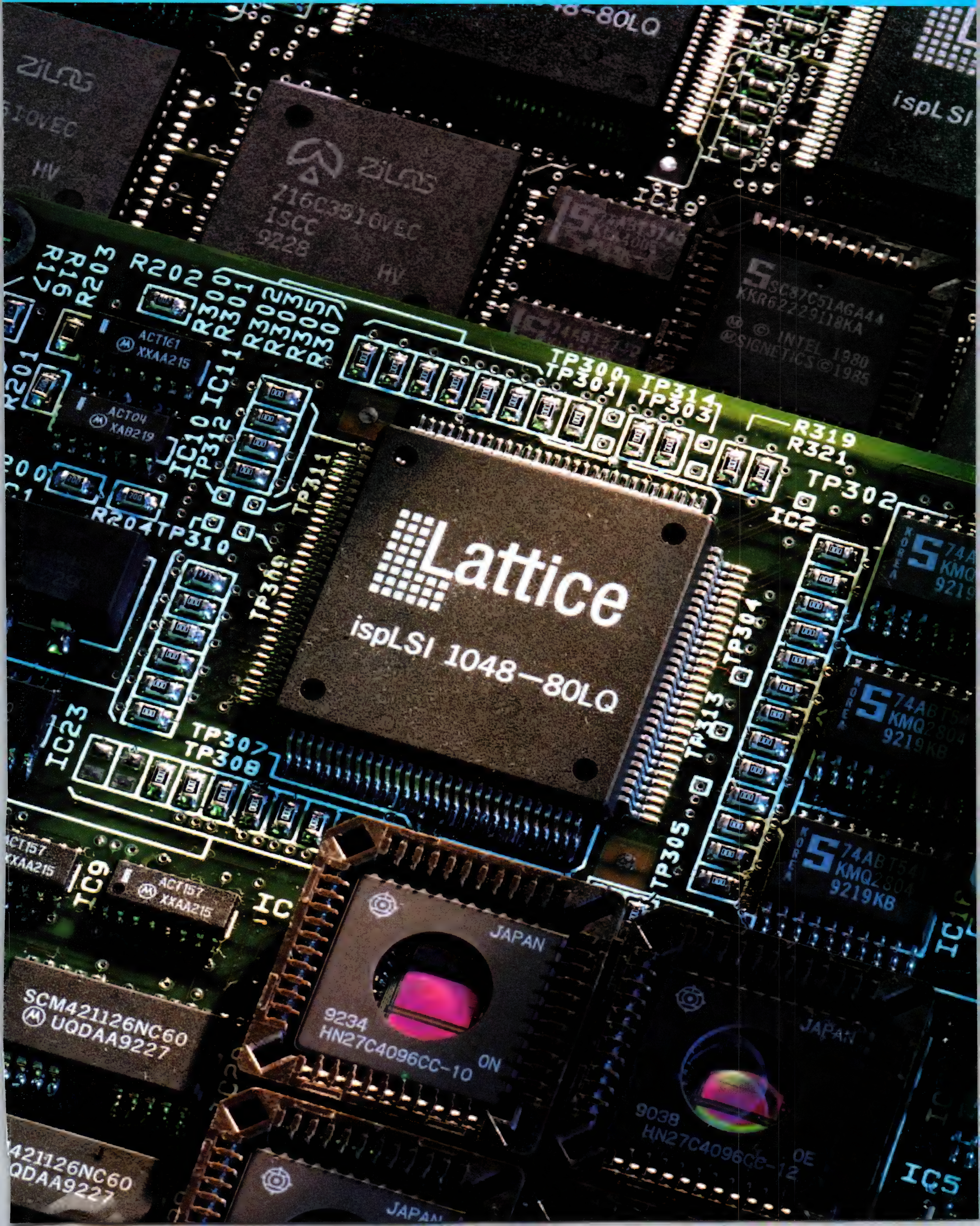


...In-System

In-System Programmability (ISP™), the ability to program and reprogram logic devices while "in-system", is the ultimate logic technology! No other technology is better for reducing time to market, while assuring the highest system quality and lowest overall cost.

In the 1970s, the bipolar PLD transformed the logic market by allowing a single component to implement custom logic functions in minutes.

In the 1980s, Lattice introduced the E^2CMOS® Generic Array Logic™ (GAL®) architecture that revolutionized the programmable logic market by providing quantum leap improvements in time to market and quality through electrical erasability, reprogrammability and 100% testability.

Now ISP is revolutionizing the system designs of the 1990s by providing an enabling technology that allows designers to define and develop systems with capabilities previously unattainable. With ISP technology, the concept of hardware as flexible and easy to modify as software becomes a reality. Hardware functions can be programmed and modified in real time to expand product features, shorten time to market, enhance product manufacturability and simplify field upgrades.

In-system programmability is an exciting concept. Lattice's ispLSI® family is the exciting reality.

	1970s	**1980s**	**1990s**
FEATURE	PAL	GAL	ISP
Design Cycle	Weeks	Days	Hours
Functional Flexibility	Good	High	Highest
Testability	Limited	100% (Device)	100% (Device & Board)
Quality	Good	High	Highest
Programming Flexibility	One Time Programmable	Reprogrammable	In-System Reprogrammable
Programming Yield	95%	100%	100% (No Programmer)
Cost of Ownership	Good	Better	Best

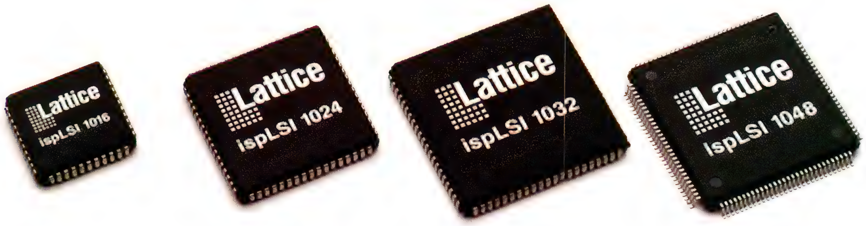
Programmability

The ispLSI Family of High-Density Programmable Logic from Lattice

The ispLSI family merges the concept of ISP with Lattice's high-performance, high-density pLSI® (programmable Large Scale Integration) architecture. The ispLSI devices are the first in-system programmable logic devices to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. With 110MHz system speed, 10ns pin-to-pin logic delays and logic densities ranging from 2,000 to 8,000 gates, they're the most powerful programmable logic components available today.

The ispLSI architecture contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provide the optimum combination of internal logic and external connections. A global, deterministic interconnect scheme ties everything together, giving predictable performance and high utilization.

The ispLSI family can implement a wide range of logic functions including registers, counters, multiplexers, decoders and complex state machines to satisfy any system design need!

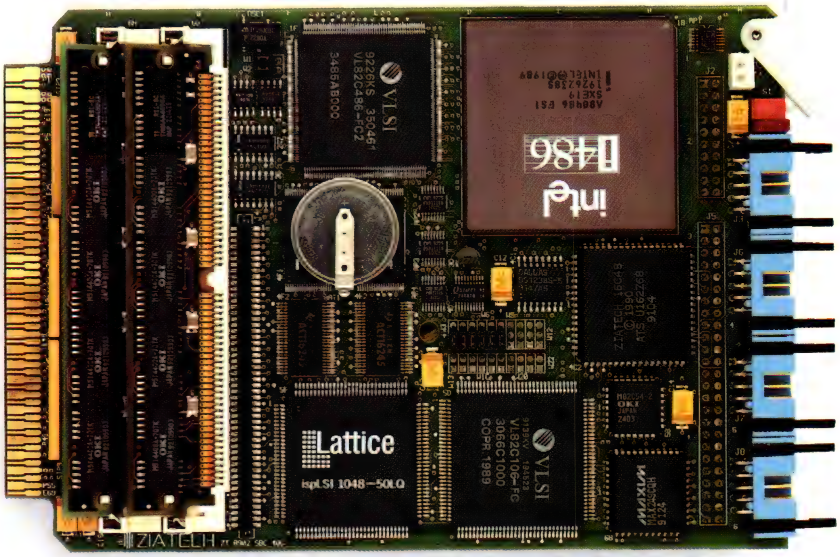


Family Overview	ispLSI 1016	ispLSI 1024	ispLSI 1032	ispLSI 1048
Density (PLD Gates)	2000	4000	6000	8000
Speed: F max (MHz)	110	90	90	80
Speed: tpd (ns)	10	12	12	15
GLBs	16	24	32	48
Registers	96	144	192	288
Inputs & I/Os	36	54	72	106
Package	44-Pin PLCC	68-Pin PLCC	84-Pin PLCC	120-Pin PQFP

ISP: Design Advantages

Designing With ispLSI Devices Provides The Fastest Time To Market.

ISP allows design, test and manufacturing engineers to reconfigure system features while the devices remain soldered on the circuit board. This capability revolutionizes design prototyping, board-level debug and system upgrades.



Small footprint 486 computer from Ziatech Corporation
(Photo courtesy of Ziatech Corporation.)

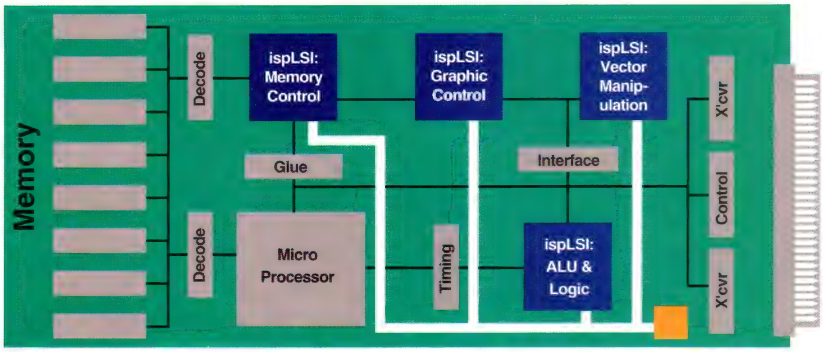
The Superior Prototyping Solution

When using ispLSI devices, the system designer can fully populate his prototype board with its major building blocks, interconnecting all functions with programmable logic. Design changes, whether they require added or modified logic, can be made in minutes using Lattice's pDS™ or pDS+™ software design tools. A 5-wire download cable from a PC or workstation to the prototype board downloads the new logic into the device(s).

Faster Debug

The system designer can also use the ispLSI devices to debug other portions of his board design. In-system programmability can be used to debug its operation more quickly by reconfiguring the ispLSI devices to force or redirect signals (e.g. clocks or control signals) to other components on the board. This saves precious time during system-level debug and translates directly into a competitive time-to-market advantage.

> *"Prototyping with the ispLSI 1032 cut more than 50% off our development and debug time. Design changes that once took half a day now are handled in minutes! Plus the flexibility and density of the architecture allowed us to introduce one of the smallest footprint 486 single-board computers on the market today."*
> *Alan Beverly, Engineering Manager, Ziatech Corporation*



Multiple ispLSI devices can be reconfigured through multiplexed signals interfaced via an edge connector, 5-post connector, microcontroller, or microprocessor.

🟦 ***ispLSI Devices***
🟧 ***isp Interface***

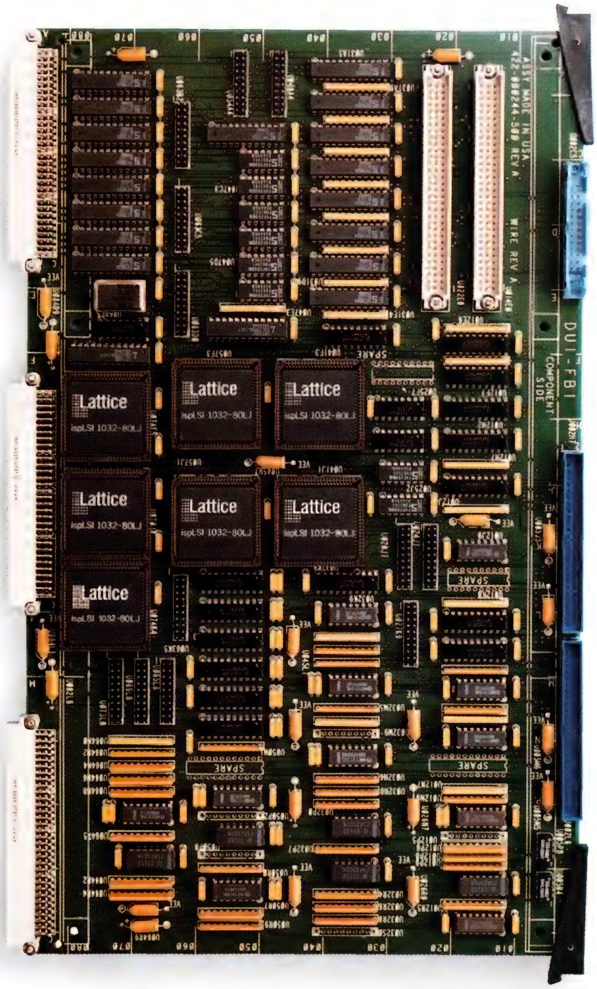
Board Reconfiguration and Field Upgrades

ispLSI devices also provide an ideal way to reconfigure boards and/or upgrade product features in the field. With conventional logic technology, a system installed at a customer location is very expensive and difficult to upgrade to the latest hardware revision, to fix hardware bugs, or enable hardware options.

With ispLSI devices, however, a simple upgrade program can be downloaded, either in the field or the factory, to reconfigure the logic (e.g. to modify memory refresh or control logic or to operate with a faster microprocessor). Updates via modem, serial link, or special ISP programming interface are possible depending on the system environment or needs.

Multi-Function Hardware

ISP also allows designers to exploit the concept of multi-function hardware. Utilizing multi-function hardware, a single hardware design can implement a variety of system-level functions through in-system programming. Multi-function hardware allows manufacturers to reduce the number of unique board designs used in a system, further simplifying the manufacturing flow.



ispLSI 1032 enables multi-function hardware on a Convex computer HDTV frame buffer interface design.
(Photo courtesy of Convex Computer Corporation)

"We decided on the ispLSI 1032 and 1024 for our Micro Channel bus interface design for several reasons: high performance, programmable clocks and resets, design flexibility down the road, and the fact that debugging the logic is a breeze!"
John McNerney, Design Engineer,
NCR Corporation

"After evaluating the ispLSI device features, we realized that our HDTV Frame Buffer Interface board design could be enhanced. Instead of limiting the design to the two original frame buffer formats, several formats could be handled using the same board by taking advantage of the in-system programmability of the ispLSI 1032."
David Harper, Senior Design Engineer,
Convex Computer Corporation

ISP: Manufacturing Advantages

ISP is not only revolutionizing the world of logic design but also dramatically transforming the world of manufacturing.

Simplified Manufacturing Flow

Today all non-ISP, high lead-count PLDs must be programmed by hand using a standard logic programmer. With the ispLSI family, devices go directly from the receiving dock to the manufacturing floor for placement on the PCB, entirely eliminating traditional stand-alone programming and mark operations. Unprogrammed ispLSI devices can be mounted directly onto the PCB without sockets or regard for the final logic configurations. Individual device configurations can be downloaded from Automatic Test Equipment (ATE) at board test.

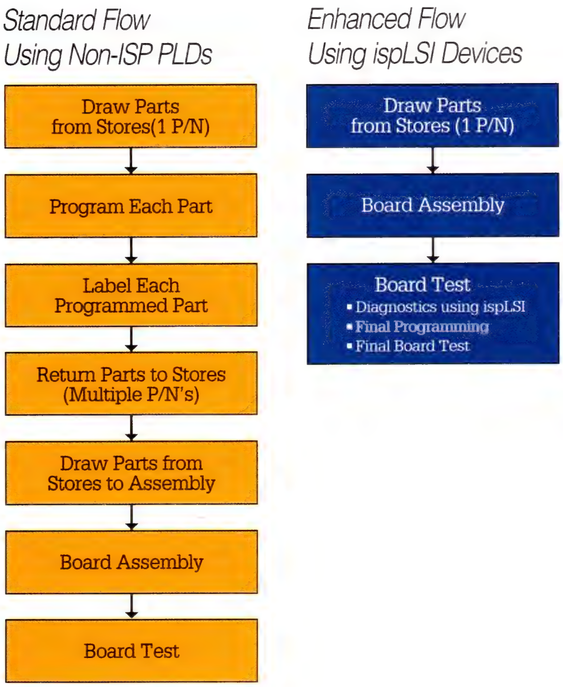
Eliminate Bent Leads

It is a difficult task to insert a high lead-count, fine-pitch device into a programming socket, program, label (or mark) and re-inventory the device without bending the delicate package leads. These bent leads ultimately result in bad solder connections, increasing the amount of board and system-level troubleshooting required. ispLSI devices solve these problems by eliminating additional handling steps during manufacturing.

Reconfigurability for Test

The ISP approach also facilitates board-level testing, increasing system fault coverage without sacrificing board resources or real estate. With ISP, a diagnostic test pattern can be temporarily programmed into the ispLSI devices to exhaustively exercise board-level functions. This allows the tester to isolate board-level problems more quickly. Once these detailed diagnostics are complete, the ispLSI devices can be reprogrammed to their normal logic configurations for final functional testing.

Manufacturing Flow



Standard Flow
Using Non-ISP PLDs
Draw Parts from Stores(1 P/N)
Program Each Part
Label Each Programmed Part
Return Parts to Stores (Multiple P/N's)
Draw Parts from Stores to Assembly
Board Assembly
Board Test
Enhanced Flow
Using ispLSI Devices
Draw Parts from Stores (1 P/N)
Board Assembly
Board Test
• Diagnostics using ispLSI
• Final Programming
• Final Board Test

> *"NEC America appreciates the benefits that the ispLSI devices represent to sectors of its manufacturing, such as reduced part types and flexible inventory."*
> *Brian Reilly, Sr. Hardware Development Engineer,*
> *NEC America, Incorporated*

> *"Northern Telecom is currently pursuing in-system programmability on our new designs due to our recognition of the cost advantages that may be obtained by removing handling steps from the manufacturing flow."*
> *John Chiang, Senior Component Engineer,*
> *Northern Telecom Limited*

ISP: Winning At The Bottom Line

ISP offers its users the opportunity to increase product value and reduce bottom-line cost simultaneously.

Added Product Value

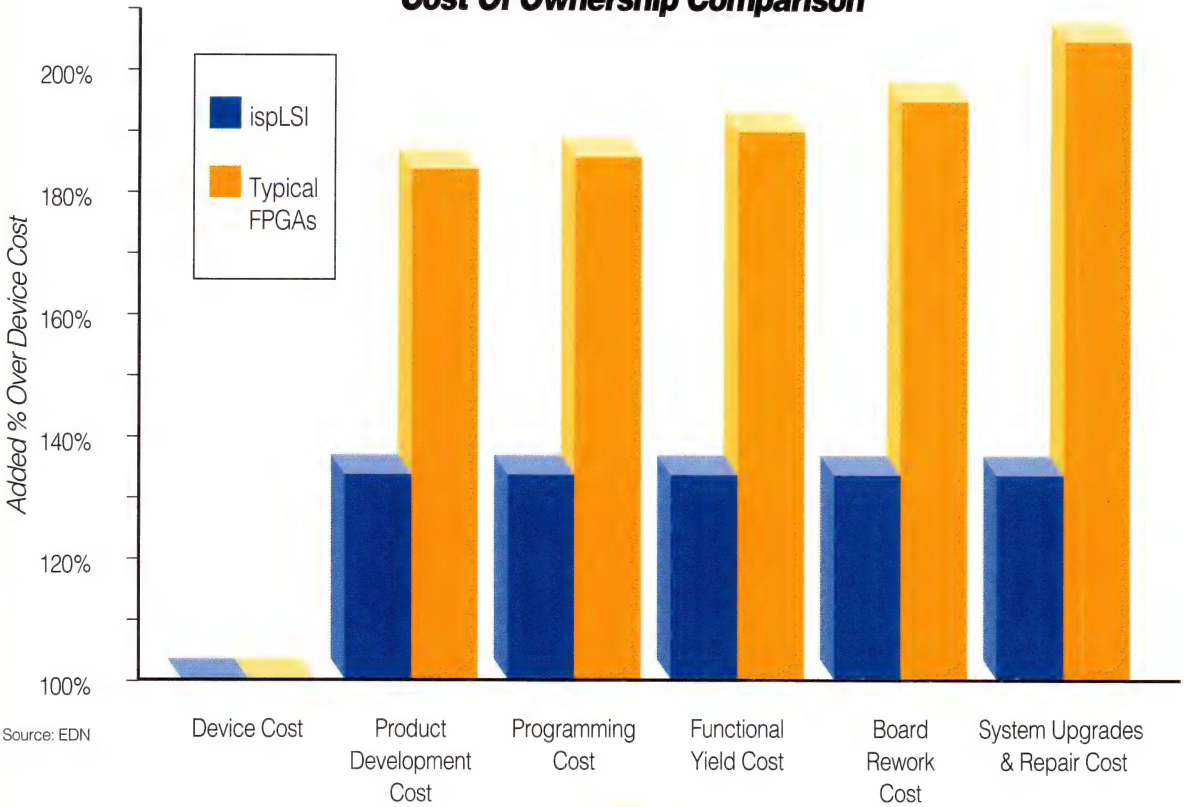
ISP allows the system manufacturer to build in added product value through the addition of unique product capabilities. Taking advantage of in-system reconfigurability will differentiate and enhance the market positioning of an ISP-based product ultimately resulting in higher sales and expanding market share.

Lowest Cost

Total cost of ownership goes far beyond the initial purchase price of components. ISP reduces costs throughout the entire life cycle of a product: product development, manufacturing, test, field maintenance and upgrades.

"Time is money! With Lattice ispLSI devices, we are able to do our development in one-fifth the time it would take with competitive FPGA solutions." William A. Long, Vice President of Engineering, Micronet Corporation, Winner of the 1990 and 1991 "Storage Product of the Year" award from MacUser Magazine

Cost Of Ownership Comparison



Source: EDN

ispLSI results in a cost savings of over one third or more when compared to typical FPGAs.

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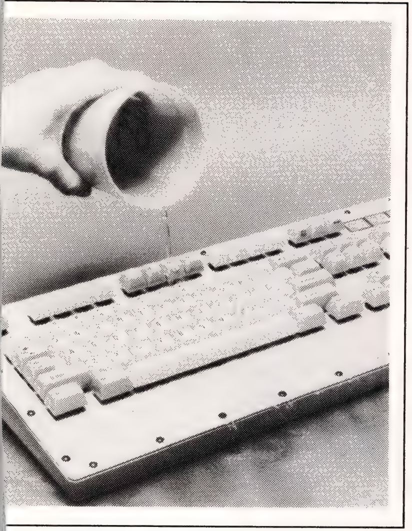


ealed keyboard. The 101SD key-
ard meets MIL-STD-202E and
EMA 4 and 13 water/moisture resis-
nce standards. The unit employs Hall-
fect, solid-state keyswitches with
lid-state encoding. The unit is format-
d with standard IBM 101 enhanced-
y layout and legends. The keyboard
s green LEDs for the Num Lock,
ps Lock, and Scroll Lock keys. The
it is UL recognized, CSA certified,
d FCC Class B certified. $953.70. De-
ery, 10 weeks ARO. **Micro Switch,**
W Spring St, Freeport, IL 61032.
one (815) 235-6600. **Circle No. 423**

ppressor chip. Housed in a 2×1.25-
n package, the LCB-0805 provides ef-
ient EMI/RFI suppression. The unit
s a 50-mA current rating and a 600Ω
pedance at 100 MHz. The device is
nstructed using multilayer technol-
y and is compatible with surface-
unt flow and reflow soldering proc-
ses. $0.135 (10,000). **Associated Com-**
nents Technology, 11575 Trask Ave,
rden Grove, CA 92643. Phone (714)
6-2645. FAX (714) 636-8276.
Circle No. 424

ermistors. WC Series positive tem-
rature (PTC) switching thermistors
ve base resistance values of 0.5 to
0Ω. The 0.5Ω PTC allows 1A to pass
rough the circuit continuously. If the
rrent exceeds 2A, the unit switches
o a high-impedance state. Voltage-
ndling capabilities and current rat-
s range from 12 to 1000V and 10 to
0 mA, respectively. $0.29 (1000). De-
ery, four to six weeks ARO. **Western**
ectronic Components Corp, 1250-A
enida Acaso, Camarillo, CA 93012.
one (805) 482-8002. FAX (805) 482-
5. **Circle No. 425**

DC/DC converters. The MAX724 and 724H have an internal 5A switch and operate from inputs of 8 to 40V and 8 to 60V, respectively. Output voltage can be set to any level between 2.5 and V_{IN} using two resistors. The reference voltage tolerance is ±2.5% max overload, line, and temperature. Quiescent current equals 8.5 mA and efficiency is 80%. The units are housed in TO-220 packages. $4.69 (1000) for the MAX724. **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 426**

Resistor networks. The MNR-34 network includes four resistors in a package measuring 0.2×0.1 in. Resistance values range from 100Ω to 330 kΩ. Power and voltage ratings are $\frac{1}{16}$W and 50V, respectively. The package has a 1.27-mm terminal pitch and features large solder pads and concave electrodes to facilitate assembly operations. $0.052 (50,000). Delivery, 10 weeks ARO. **Rohm Corp,** 3034 Owen Dr, Antioch, TN 37013. Phone (615) 641-2020, ext 116. FAX (615) 641-2022. **Circle No. 427**

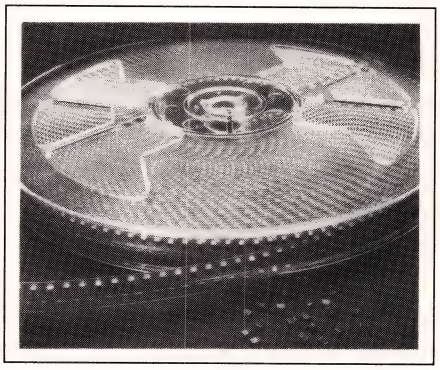
DC/DC converters. NT Series converters develop a 25 to 30W output in a 2.02×1.62×0.55-in. package. All three of the single-output units have transient overvoltage suppressor diode protection on the output terminal. Overcurrent and overtemperature protection are also standard. Efficiency ranges to 86%, and input-output isolation equals 1544V dc. $63.45 (OEM qty). **Calex Mfg Co Inc,** 2401 Stanwell Dr, Concord, CA 94520. Phone (800) 542-3355; (510) 687-4411. FAX (510) 687-3333. **Circle No. 428**

Surface-mount inductors. The 40 standard models in the BCL Series of surface-mount inductors are designed for high-current applications. Inductance values range from 0.01 to 1000 μH. Standard tolerance equals ±20% for values of 0.01 to 0.82 μH and ±10% for values of 1 to 1000 μH. Tolerances of ±5 and ±3% are also available. $0.35 (1000). Delivery, stock to six weeks ARO. **Beckman Industrial Corp,** 4141 Palm St, Fullerton, CA 92635. Phone (714) 447-2345. **Circle No. 429**

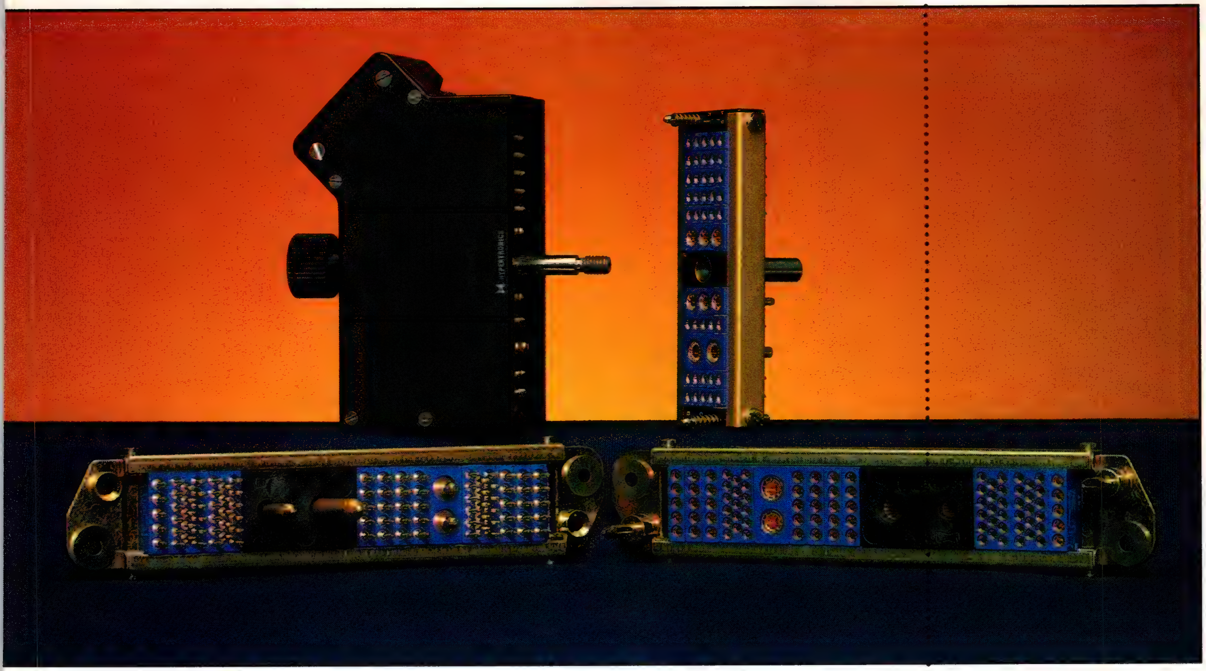
RF transistors. The BFG540, BFG10, and BFG11 combine to produce a complete 1.9-GHz amplifier that can deliver 500 mW of RF output and operate from supply levels of 3V. The surface-mount packages can be easily assembled on FR4 laminate pc boards. The 3-stage lineup can achieve a 26-dB-typ power gain at 1.9 GHz and operate at 40% efficiencies. With a 3.3V supply, the power gain equals 25 dB min and the available power output is 400 mW. BFG540, $0.40; BFG10, $0.93; BFG11, $1.24 (100,000). Delivery, eight to 10 weeks ARO. **Philips Components,** 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762. **Circle No. 430**

Philips Components, Marketing Communications Dept, Bldg BA, 5600 MD, Eindhoven, The Netherlands. Phone local office. **Circle No. 431**

DIN connectors. The Omnigrid 2.5-mm connector line is based on the IEC 917 metric practice, which uses system units (SU) in increments of 25-mm long as standard. The smallest module is 1SU, and it can have 35 signal contacts, two coaxial contacts, or two power contacts for currents as high as 35A each. Modules as large as 10SU are available with as many as 475 contacts. The system uses standard 0.025-in. square pins. The connectors are designed for operation at 800-Mbps transmission rates. $0.11 per mated circuit (25,000) for a 9SU model. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532. Phone (708) 969-4550. FAX (708) 969-1352. **Circle No. 432**



Chip inductors. ACCU-L Series surface-mount inductors are packaged as 0805 chips. Units have inductance values of 2.7 to 15 nH with tolerances of ±0.5 nH and ±5%. Based on thin-film multilayer technology, the units have SRFs (series resonant frequencies) of 2200 to 10,000, Q of 36 to 80, and dc resistance of 0.08 to 0.2Ω. The inductors are designed for applications between 100 MHz and 2 GHz. $0.48 (10,000). **AVX Corp,** Box 867, Myrtle Beach, SC 29577. Phone (803) 448-9411. FAX (803) 626-2442. **Circle No. 433**



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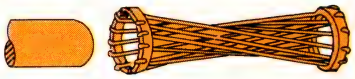
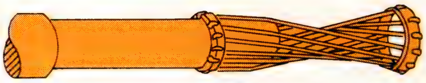
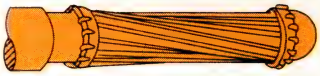


Wire sleeve before insertion of pin.



Pin partially inserted into sleeve.



Pin completely inserted into sleeve.

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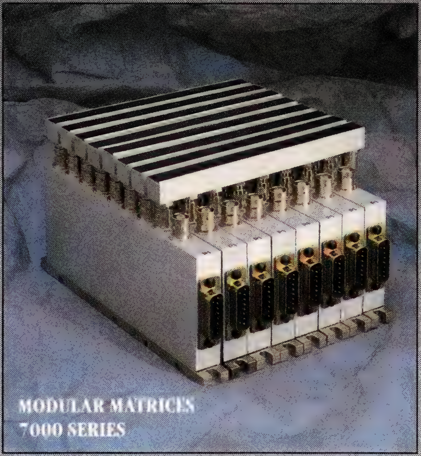

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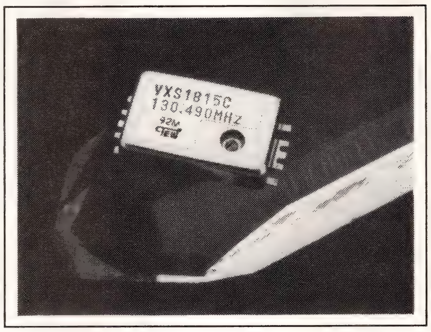
CIRCLE NO. 118

DIP adapter. The XX-350681-10 SOIC-to-DIP adapter permits a small-outline integrated circuit to be surface mounted to the top of a DIP socket for attachment to a through-hole pc board. It is available in versions with 8 to 28 pins (where XX equals the number of pins) on 0.100-in. centers. $4.38 (1000) for a 24-pin model. Delivery, stock to six weeks ARO. **Aries Electronics Inc,** Box 130, Frenchtown, NJ 08825. Phone (908) 996-6841. **Circle No. 466**



Crystal oscillator. The VXS1815C voltage-controlled crystal oscillator develops a sine-wave output in the 60- to 150-MHz range. The units operate from a 5V supply and feature a ±10-ppm frequency stability over a -20 to +75°C. Output impedance equals 50Ω and suppression measures -20 dB. RF output equals -5 dBm±3 dB. $20 (10,000). Delivery, 12 weeks ARO. **TEW North America,** 5903-B Peachtree Ind Blvd, Norcross, GA 30092. Phone (800) 762-0420. FAX (404) 441-3076. **Circle No. 467**

LED lamps. The SLA-560 Series features red and green lamps that do not compromise brightness over their 40° viewing angle. The red unit provides a luminous intensity as high as 1100 mcd at 20 mA forward current, and the green lamp emits as much as 360 mcd. The two lamps can be combined to produce a yellow-colored lamp. Green lamp, $0.06; red lamp, $0.125 (1000). Delivery, eight weeks ARO. **Rohm Corp,** 3034 Owen Dr, Antioch, TN 37013. Phone (615) 641-2020, ext 131. FAX (615) 641-2022. **Circle No. 468**

LEDs. Series 5379K LEDs feature a semiround or convex diffused lens that concentrates the emitted light so that its intensity is 8 to 10 times higher than a typical 2.5×5-mm rectangular LED—24 mcd vs 3 mcd at 20 mA for a typical rectangular GaAlAs red LED. The series includes red, green, yellow, and orange colors. The units are packaged in bulk, folded tape, or tape-and-reel. $0.115 (10,000). **I I Stanley Co Inc,** 2660 Barranca Pkwy, Irvine, CA 92714. Phone (800) 533-5331; (714) 222-0777. FAX (714) 222-0555. **Circle No. 469**

Crystal oscillator. Model CO-718SL2 oven-controlled crystal oscillators are housed in a 2×2×1.25-in. package and develop outputs in the 4- to 2000-MHz range. Stability is $\pm 5\times 10^{-9}$ over a 0 to 50°C range and $\pm 5\times 10^{-10}$/day aging. $436 (100) for a 5-MHz version. Delivery, 14 weeks ARO. **Vectron Laboratories Inc,** 166 Glover Ave, Norwalk, CT 06856. Phone (203) 853-4433. FAX (203) 849-1423. **Circle No. 470**

Solid-state relays. Available in 8-pin DIP and surface-mount versions, the LH1531 and LH1532 Dual 1 Form A relays can switch as much as 350V ac or dc at currents of 110 mA. The 1531

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CIRCLE NO. 119

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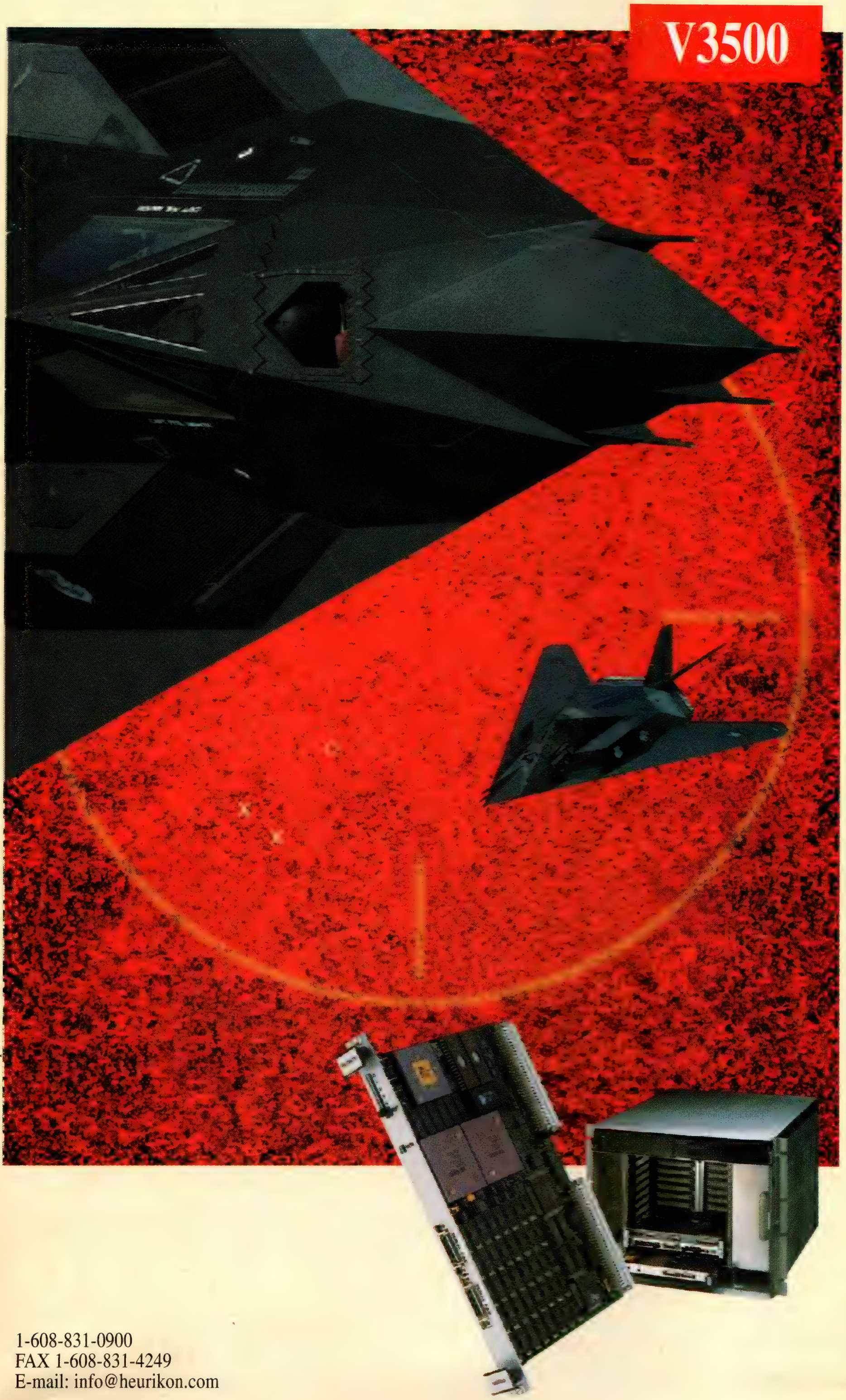

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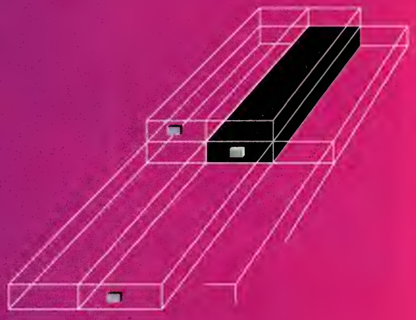
			Charging Current (mA)	Time (Hrs.)	L (mm)	W (mm)	T (mm)	
KF-A600	1.2	600	60	14-16	67.0	17.0	6.1	23
KF-A900	1.2	900	90	14-16	67.0	17.0	8.1	30
KF-A1200	1.2	1200	120	14-16	67.0	17.0	10.3	38
KF-B600	1.2	600	60	14-16	48.0	17.0	8.1	21
KF-B400	1.2	400	40	14-16	48.0	17.0	6.1	16

CIRCLE NO. 121



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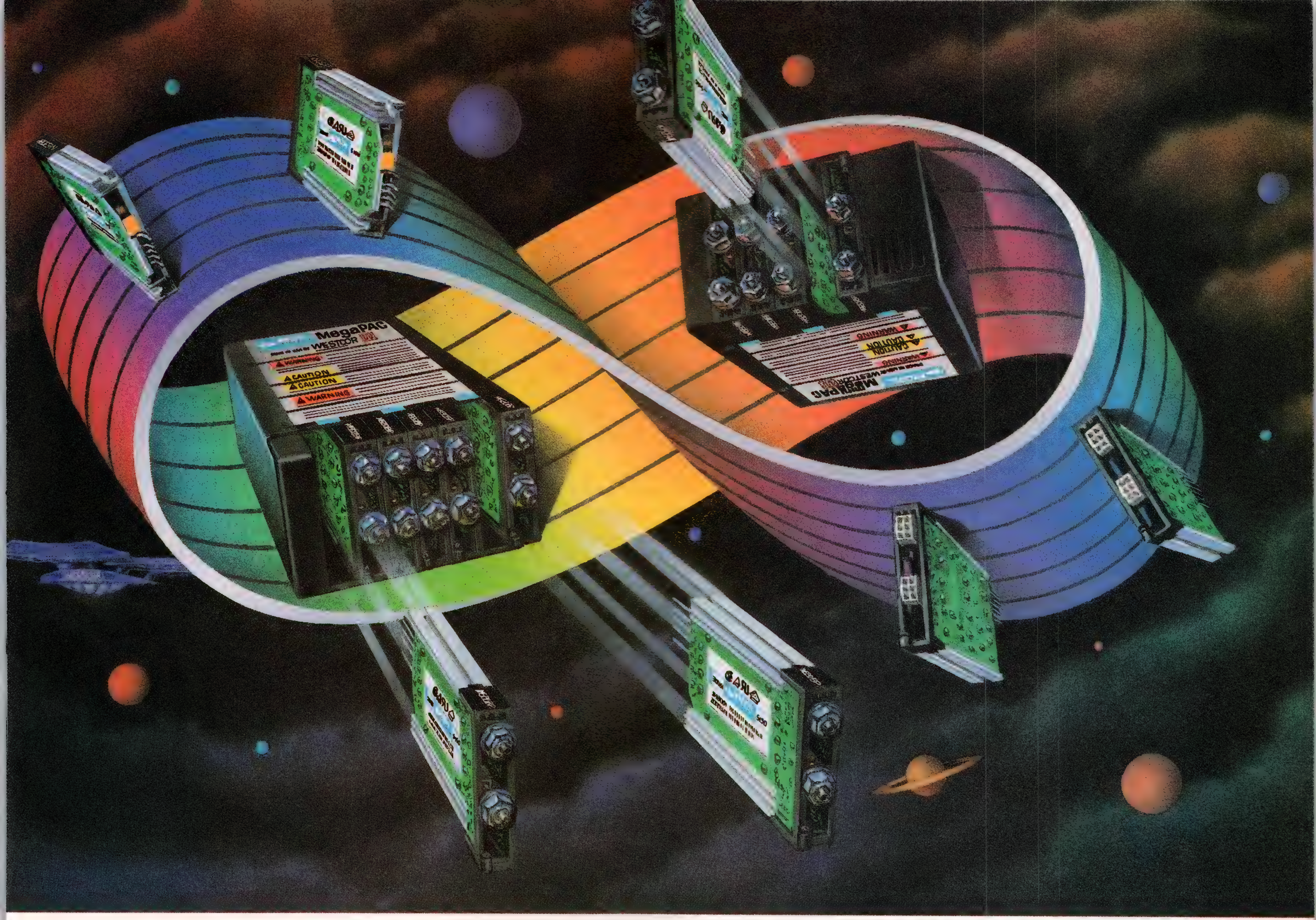

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- 120/240 VAC strappable
- 120/240 autostrapping universal input ***NEW! Automatically senses line voltage and straps power supply accordingly.***
- 85-264 VAC universal input with power factor correction ***NEW! Meets IEC 555.***

Output Options

- Up to 1600 watts total
- Up to 100 or up to 200 watts per output
- 1-16 outputs, isolated & fully regulated
- 1 to 95 VDC

ModuPAC slide-in converter assemblies:

- Standard—one output, up to 200 watts
- ***NEW* DualPAC**™ —two outputs, up to 100 watts each
- ***NEW* TachoPAC**™ —for fast transient response to high-speed load changes
- ***NEW* RamPAC**™ —for very low noise
- ***NEW* VXI Option**—for low noise and low ripple to meet instrumentation standard VXI

Family Options

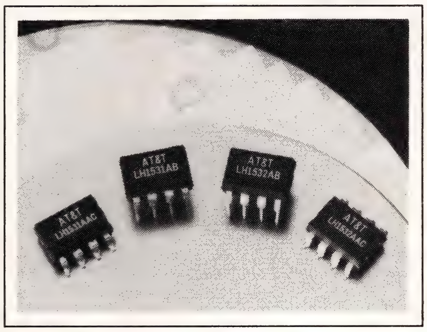
- DC OK (Power Good)—TTL signal high when output is ≥90% of nominal
- Trim range ±10% or 40-110% of nominal
- Industrial or military grade modules
- Hardwired local sense
- Enable/Disable—TTL signals inhibit or enable each output; includes one-pin global shutdown

Component Solutions For Your Power System

VICOR

Vicor Corporation • 23 Frontage Rd., Andover, MA. 01810 USA • TEL: (508) 470-2900 • FAX: (508) 475-6715
Vicor GmbH • Tel: +49-89-329-2763 • Fax: +49-89-329-2767 • **Vicor Far East** • Tel: +886-2-9188240 • Fax: +886-2-9132982

CIRCLE NO. 122



features an integrated V_{BE} multiplier, which provides very fast turn-on; the 1532 uses on-chip current-limiting circuitry to provide protection from voltage surges. Both parts feature 3750V ac input-to-output isolation. $2.96 (10,000) for the DIP version. **AT&T Microelectronics,** 555 Union Blvd, Dept 500404200, Allentown, PA 18103. Phone in US, (800) 372-2447, ext 149; in Canada, (800) 553-2448, ext 149.

Circle No. 471

Zinc die cast and high axial strain relief
Custom molded
Spring latch
Thumbscrew

- Unique, patented shielding technique presents the ultimate RF tight system.

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Many of the biggest names in the computer industry have sought our advice on SCSI problems. That's because we at Harbor Electronics are recognized experts. And we have the experience to develop sophisticated engineering solutions to proprietary problems.

Our involvement in both active and passive products means Harbor is a knowledgeable source for a wide range of SCSI devices. And since we're the largest producer of SCSI interface assemblies, our prices are globally competitive.

So if you're starting a new project and you're facing a potential problem involving SCSI-1, 2 or 3 molded cable assemblies or terminators, and you want expert advice, call Harbor Electronics at 203-438-9625.

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We put perfection first.

650 Danbury Road, Ridgefield, CT 06877. (203) 438-9625

Thermistors. The Uni-Chip glass-encapsulated negative-temperature-coefficient thermistors are available with resistance values of 1 kΩ to 5 MΩ. Resistance tolerance ranges from 1 to 10%. The devices are also available in versions featuring 1°C accuracy in five standard resistance values ranging from 10 kΩ to 100 kΩ. The devices are housed in a DO-35 package that can withstand temperatures from -60 to +300°C. $0.42 (5000) for a 10% unit. **Fenwal Electronics,** 450 Fortune Blvd, Milford, MA 01757. Phone (508) 478-6000. FAX (508) 473-6035.

Circle No. 472

Connector kits. These kits are designed to simplify customer testing of different elastomeric elements. Each consists of an elastomeric element, two pc boards, a board-to-board connector, hardware, and complete testing instructions. Kits are available for silver STAX HP, nickel Matrix MOE MN (metal-on-elastomer), and gold Wrap MOE WG elements. A kit is also available for military applications. $30 to $65. **Elastomeric Technologies Inc,** 2940 Turnpike Dr, Hatboro, PA 19040. Phone (215) 672-0787. FAX (215) 672-4633.

Circle No. 473

DC/DC converters. CP200 converters develop a 280W output over a -20 to +85°C operating range. The units accept inputs of 18 to 36V and output values of 5, 5.2, 12, 15, 24, or 28V with respective current ratings of 40, 38, 20, 16, 11, and 10A. All models can be paralleled, and they include standard TTL-compatible on-off logic for use in standby or N+1 redundant modes. A Sync pin is also provided. From $175 (OEM qty). **Abbott Electronics,** 2727 S La Cienega Blvd, Los Angeles, CA 90034. Phone (310) 202-8820. FAX (310) 836-1027.

Circle No. 474

Optical encoder. The 25/04S absolute encoder has a 17-bit resolution and a ±3.2 arc-sec rms accuracy. Novel zero-hysteresis circuitry eliminates dead-band so there's no error due to bidirectional operation. Data update rate equals 1 MHz. Natural binary or Gray code output is available in either parallel (3-state TTL) or serial (EIA/RS-422) format; a parity bit is standard. From $1200. **Teledyne Gurley,** Box 88, Troy, NY 12181. Phone in US and Canada, (800) 759-1844; (518) 272-6300. FAX (518) 274-0336.

Circle No. 475

All Packed And Ready To Go...Anywhere!

If you need up to 5 kV of first class DC voltage at 300 watts and a power supply design that complies with IEC/CSA 950 and UL 1950 international standards, the MR Series of high voltage modules are just your ticket… at a business class price! Five models with full scale outputs from 1 kV to 5 kV, ripple less than 0.02% RMS of rated voltage, voltage regulation better than 0.005% from short circuit to rated voltage, and a rapid 2 ms response to a 50% load transient.

Overload protection, including protection from arcs and shorts, is automatic with a crossover from constant voltage regulation to current control. Current control can be user-configured for constant current regulation … better than 0.1% of rated current from short circuit to rated voltage … or current trip, to turn the output off in the event of an overload. Provisions for an external safety interlock and TTL enable/disable. Local and remote control and external monitoring are standard, of course.

Choice of output connectors. SHV connector for RG-59 cable, shown on left, or Alden connector for unshielded silicone-covered wire.

Measuring just 3.38″ (85 mm) H x 7.25 (184) W x 16 (406) D and weighing less than 11 lbs (5 kg)…thanks to Glassman-featured air insulation…the MR Series travels light. And it's fully supported by a three year warranty and factory service available on 3 continents.

Make a reservation today with your local Glassman office or distributor for all the details on the new MR Series, as well as 14 other series of high voltage power supplies, covering 1 kV to 500 kV, 15 W to 15 kW.

Innovations in high voltage power supply technology.

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Glassman High Voltage, Inc.
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U.S.A.
Telephone: (908) 534-9007
TWX: 710 480-2839
FAX: (908) 534-5672

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Glassman Europe Limited
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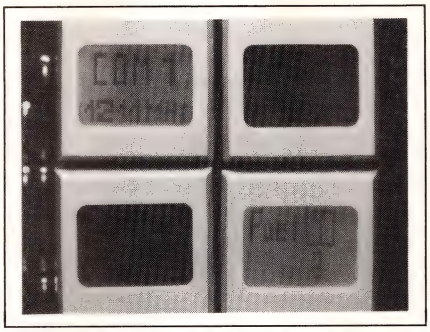
Intec 2
Wade Road
Basingstoke
Hampshire RG240NE
England
Telephone: (0256) 810808
FAX: (0256) 810815

GLASSMAN JAPAN
Glassman Japan High Voltage Limited
Taira Building
1-17, Taira 1-chome
Miyamae-ku, Kawasaki 216
Japan
Telephone: (044) 877-4546
FAX: (044) 877-3395

CIRCLE NO. 124

Pushbutton switch. The LC Series switch has a built-in programmable LCD. The 12.5×17.5-mm screen will display 16×32 pixels and can be programmed for alpha or numeric characters, graphics, and animation. The unit is also available with red or green backlighting. The switch is controlled from a clock-data bus, which can supply data to as many as 255 switches. The unit refreshes its display from within and places no demands on CPU computing time. It is pc-board mountable and meets IP 43 splash-proofing requirements. Unit without backlighting, $28.40; unit with backlighting, $37.47. **Preh Electronic Industries,** 470 E Main, Lake Zurich, IL 60047. Phone (708) 438-4000. FAX (708) 438-5522.

Circle No. 337



DC/DC converters. The TWR Series is available in 2×1×0.375-in. packages, which have 8 to 11W outputs; the 2×2×0.45-in. packages are rated for 12 to 15W. Input voltage for all units ranges from 4.7 to 72V. All converters have a 5V main and either ±12 or ±15V auxiliary outputs. Efficiency ranges to 82%, and operating range spans −25 to +105°C. The 2×1×0.375-in. package, $69; 2×2×0.45-in. package, $80 (100). **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356.

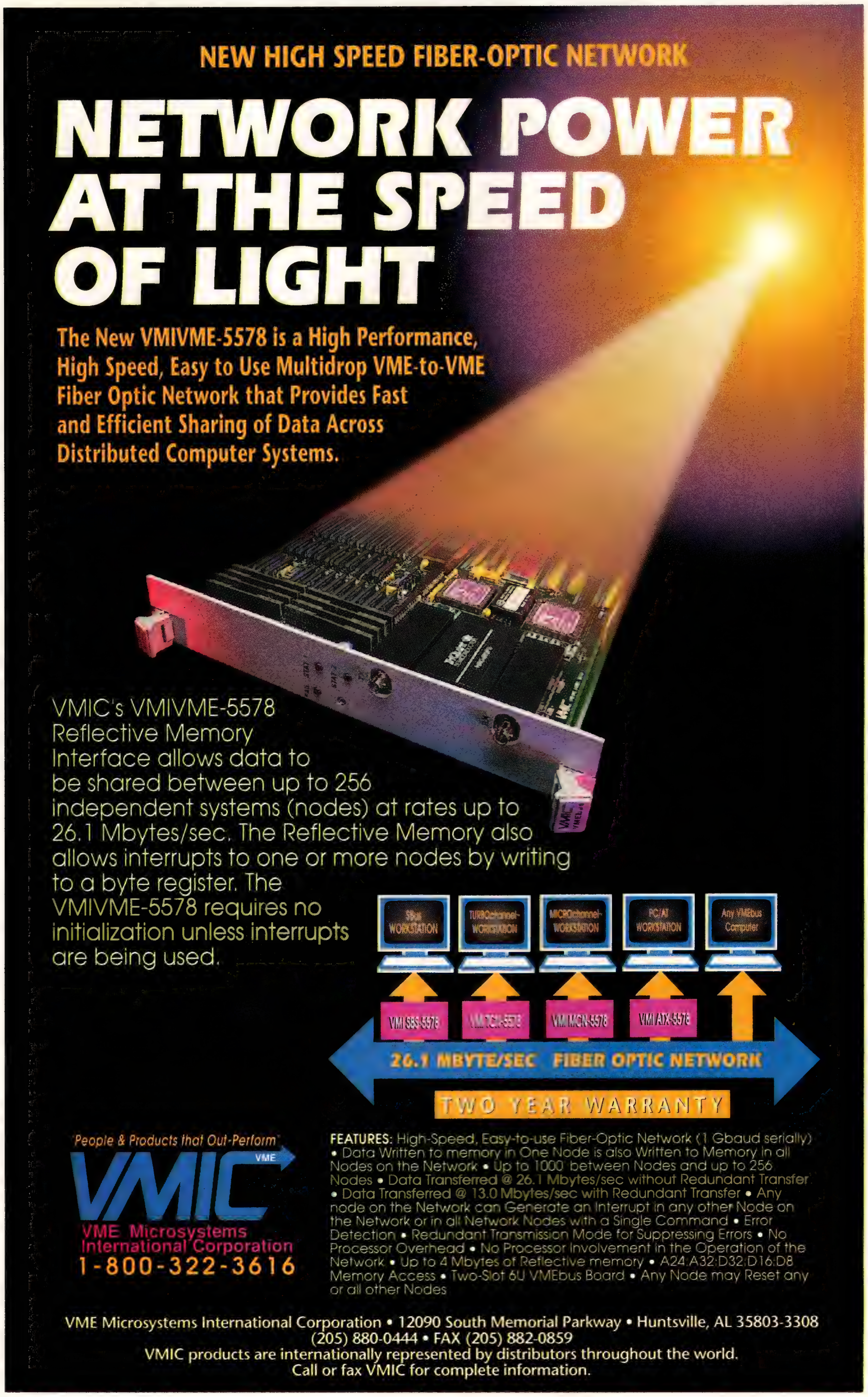
Circle No. 477

Adapters. These adapters are emulator pod rotators that allow engineers to access a PGA device on a board under test. The units rotate the probe 90° in either direction. If one 90° is not enough, the user can stack two units to achieve 180° rotation. Operating frequency equals 33 MHz min. Specific solutions are available for many µPs on the market. Rotators that are wired one-to-one are available for popular pin counts ranging from 121 to 324. $364 to $972. **Emulation Technology Inc,** 2344 Walsh Ave, Building F, Santa Clara, CA 95051. Phone (408) 982-0660. FAX (408) 982-0664. TLX 981866.

Circle No. 478

Projection panel. The Professional Presenter DP-2000 is an active matrix projection panel. It sits on top of an overhead projector and allows an individual to present digitized information directly from an electronic source to a projection screen. The unit can project computer images from a palette of 16.7 million colors for true 24-bit resolution. It also provides 32,000 colors from live video or scanned sources and works with 256-color VGA graphics cards. The unit can project anything from text and graphics to photography and animation. $5995. **Polaroid Corp,** 575 Technology Square, Cambridge, MA 02139. Phone (800) 225-1618; (617) 577-2000.

Circle No. 479


NEW HIGH SPEED FIBER-OPTIC NETWORK

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The New VMIVME-5578 is a High Performance, High Speed, Easy to Use Multidrop VME-to-VME Fiber Optic Network that Provides Fast and Efficient Sharing of Data Across Distributed Computer Systems.

VMIC's VMIVME-5578 Reflective Memory Interface allows data to be shared between up to 256 independent systems (nodes) at rates up to 26.1 Mbytes/sec. The Reflective Memory also allows interrupts to one or more nodes by writing to a byte register. The VMIVME-5578 requires no initialization unless interrupts are being used.

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CIRCLE NO. 125

BETTER WAYS FOR GATE ARRAYS

How does Orbit slash per-unit cost on quantities as low as 100 pieces?

WHY PAY FOR AN FPGA

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For Netlis

ANY VOLUMES

NO VOLUME commitment

LOW TO NO NRE'S

CONVERT @ LOW QUANTITIES

LOW POWER

Slash the cost per unit of FPGAs.

Now, with our new Encore! netlist conversion service, it makes economic sense to turn your expensive FPGAs into inexpensive ICs.

The following table shows the Encore! packages that are available.

Encore Base	44	68	84	100	144	176	208
# of Gates	660	2,000	4,000	6,000	14,000	22,000	32,000
Packages	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP	160 PQFP	208 PQFP
	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP	160 PQFP
PLCC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP
PQFP	16 SOIC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP
SOIC					44 PLCC	68 PLCC	84 PQFP
						44 PLCC	68 PQFP

Also available TQFP and PGA packages.

In a matter of a few weeks you see parts from your converted netlist. Because Orbit Semiconductor can turn around prototypes and production quantities faster than anyone else in the industry.

So you cut your cost-per-unit very quickly. And since your NRE is low, your paybacks are fast.

- Convert FPGA netlists for low NRE
- Get prototypes in as little as 3 weeks
- Die sizes allow for smaller packages
- Move quickly into production

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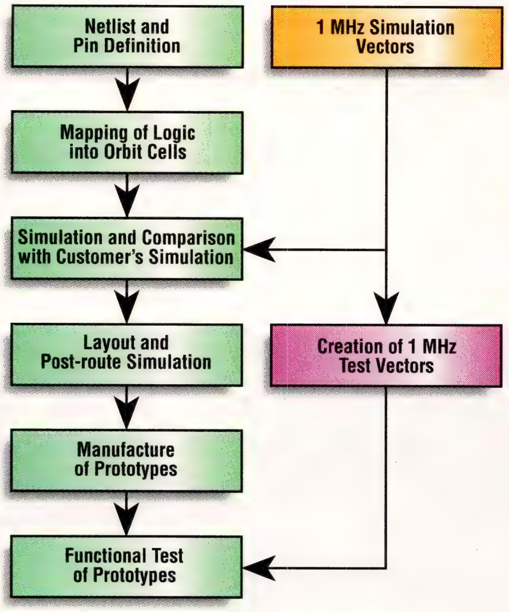
Conversion.

HIGH PERFORMANCE

3v/5v

PICK YOUR PACKAGE


Netlist and Pin Definition
1 MHz Simulation Vectors
Mapping of Logic into Orbit Cells
Simulation and Comparison with Customer's Simulation
Layout and Post-route Simulation
Creation of 1 MHz Test Vectors
Manufacture of Prototypes
Functional Test of Prototypes

Encore! also converts your gate array netlists. Affordably.

So you're no longer tied to the fab that came with the library-you can use Orbit Semiconductor for production, to meet sudden demand, or as a second source.

Here's what we need to get started:

- FPGA or gate array netlist
- Pin description file that maps package pins to netlist I/O pins
- 1 MHz simulation showing all pins in a print-on-change format
- Above files should be supplied in ASCII format

For more information on converting your FPGAs and gate arrays with Encore! contact Technical Marketing at 1215 Bordeaux Drive, Sunnyvale, CA 94089. Phone (408) 744-1800, FAX (408) 747-1263.

Or call us at (800) 331-4617. In California (800) 647-0222.

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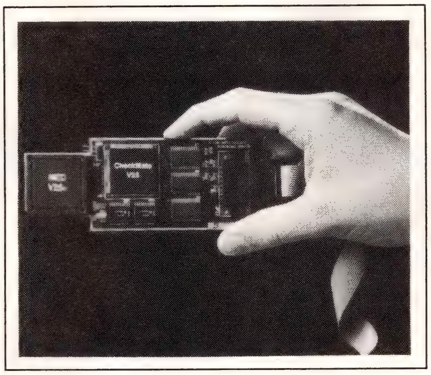
What others promise, we guarantee.

CIRCLE NO. 126

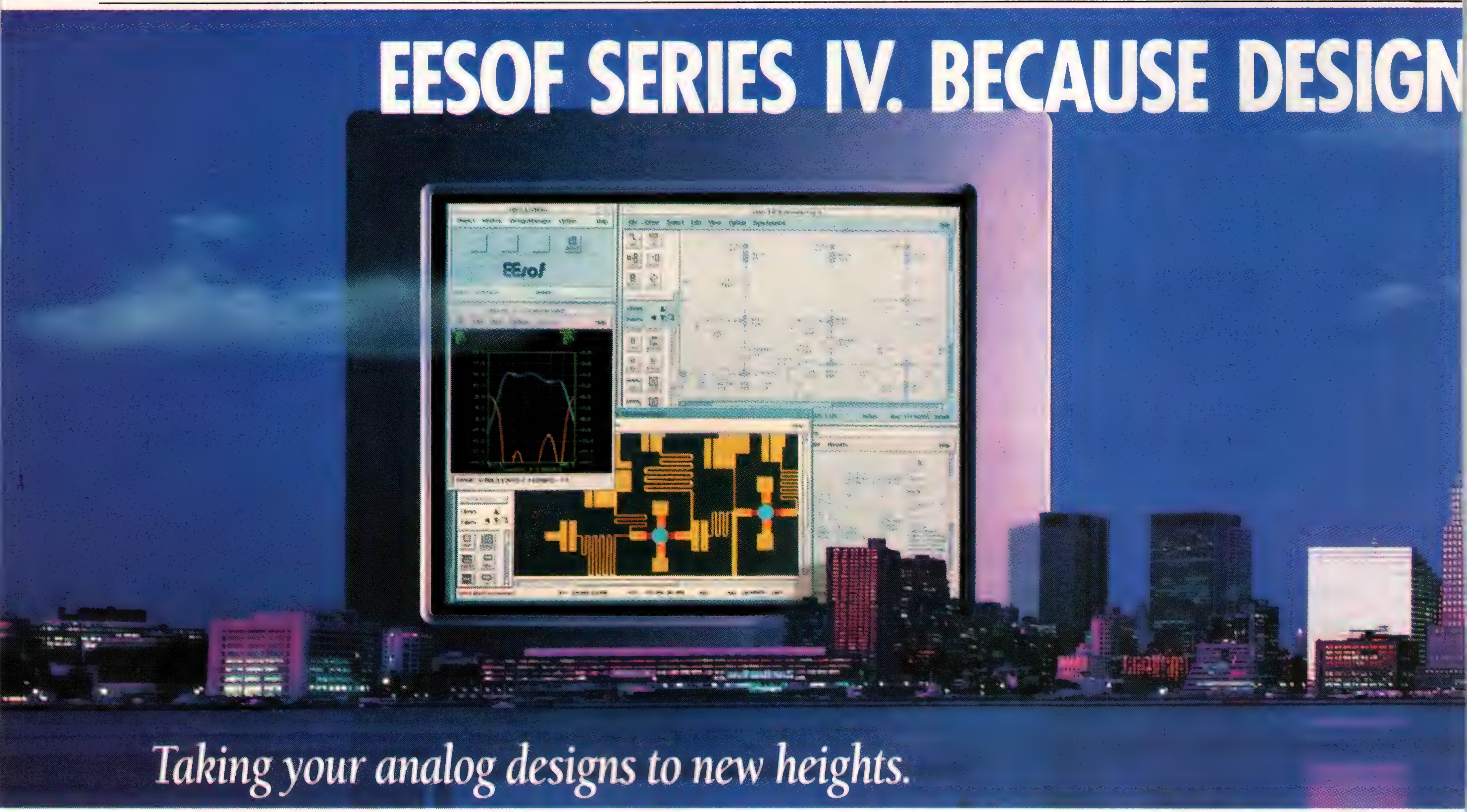
Math package for analog/digital scopes. Math+ software is a $500 option for the PM 338X and PM 339X scopes. The option performs such functions as differentiation and integration of waveforms, calculation of FFTs, construction of histograms, generation of envelopes, and pass/fail testing. The option also allows labeling of the Y axis in engineering units; the scale factor is a floating-point number with units selectable among 10 quantities. From less than $5000. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. **Circle No. 480**
Philips Test and Measurement, Building TQIII-4, 5600 MD Eindhoven, The Netherlands. **Circle No. 481**



In-circuit emulator for V25 and V25 Plus. The $5995 Checkmate-V25 ICE is about the size of most emulators' probes. It operates at 10 MHz with no wait states and includes the Paradigm Debug source-level debugger. The ICE communicates with the host CPU at 10 Mbps; it offers a hardware event system that can trigger a breakpoint or trace on address, data, or instruction status. The trace memory depth is 1k frame. The emulator does not use address or I/O space in the target, nor does it use the target interrupt table or stack space. **Checkmate Systems,** Box 3361, Redmond, WA 98073. Phone (206) 869-7211. FAX (206) 861-3647. **Circle No. 482**

50-MHz waveform generators. Models 80 ($2695), 81 ($3495), and 85 ($3995) produce sine, haversine, square, triangular, and pulse waveforms to 16V p-p in triggered, gated, gated burst, amplitude modulated, frequency modulated, voltage-controlled frequency, and phase-locked offset modes. The 80 and 85 provide logarithmic and linear frequency sweeps; the 81 offers externally controlled pulse-width modulation; and the 85 incorporates a 300k-sample/sec 12-bit waveform digitizer. **Wavetek Corp,** 9045 Balboa Ave, San Diego, CA 92123. Phone (619) 279-2200. **Circle No. 483**

Universal 225-MHz counter. The 53131A, which is based on the continuous measurement technology of the vendor's modulation-domain analyzers, gathers thousands of times more data than conventional reciprocal counters do and uses real-time signal processing to make high-resolution measurements at high speed. The counter offers 500-psec single-shot, time-interval resolution and can place 200 fully formatted measurements per sec on the IEEE-488 bus. An optional channel extends the counter's range to 3 GHz. $1675. Delivery, 10 to 12 weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 484**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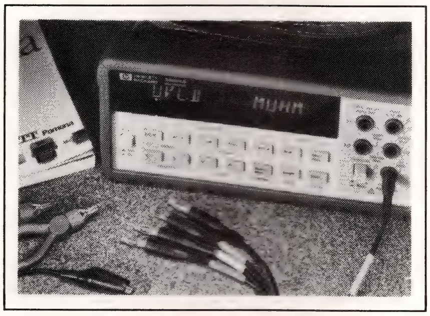
Interconnect parameter analyzer. The IPA 310 combines the fixturing, acquisition, and analysis capabilities needed to accurately model the high-frequency behavior of connections—for example, the bonding wires within a multichip module. The system, which includes an i486-based PC, is built around the vendor's 11801A digital sampling scope with time-domain-reflectometer (TDR) plug-ins. Probe stations are available for pin-grid arrays, quad flatpacks, and multichip-module packages. The analysis software corrects for multiple reflections in the TDR waveform. From $74,950; delivery 8 weeks, ARO. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 485**



Kelvin clip test set. The 5940 is intended for milliohm measurements using high resolution (6½-digit) multimeters. The set includes four measurement leads (two force; two sense) terminated in a pair of gold-plated Kelvin clips, and a fifth lead for guard or ground terminated in a miniature alligator clip. All leads are bundled in a 24-in.-long sheathed assembly that ends in gold-plated banana plugs for connection to the meter. The set is rated at 50V and 5A max. $120. **ITT Pomona,** Box 2767, Pomona, CA 91769. Phone (909) 469-2900. **Circle No. 486**

Moderately priced combinational pc-board tester. The L321 performs 20-MHz digital in-circuit, functional, and boundary-scan testing. The system, which occupies a floor area of 1.7m^2 and is available with as many as 3024 test points, integrates SuperFast Analog, VXI, and IEEE-488 instruments. Pattern memory depth behind each pin is 64k bits. Each test pattern includes 256 unique timing sets to locate edges and specify cycle time. A 1500-pin system costs $420,000. **Teradyne Inc,** 321 Harrison Ave, MS L-57, Boston, MA 02118. Phone (617) 422-3567. FAX (617) 422-3440. **Circle No. 487**

Extendible buffer/error memory for memory-device test system. The EBEM option for the vendor's Genesis IIex memory test systems uses eight µPs to concurrently process and analyze errors detected during device testing. There are three configurations of the 2-board option: an 18-Mbit version costs $16,000; a 36-Mbit version costs $21,000; and a 72-Mbit version costs $30,000. **Megatest Corp,** 880 Fox Lane, San Jose, CA 95131. Phone (408) 437-9700. FAX (408) 453-3476. **Circle No. 488**

500-MHz VLSI IC test system. The T6691 permits testing of devices with as many as 1280 pins. Its test patterns can include 5 edges per cycle with 4-psec resolution. Pattern depth is 8M or 16M 3-bit patterns per pin. Driver and

Series IV is Motif compliant. It easily fits into your UNIX network and integrates efficiently with general purpose EDA frameworks. ❖ Join the more than 2,000 companies in over 30 countries who use EEsof software. Call 818-879-6451 or 800-343-3763 (in the U.S.) for a brochure. Series IV—the high-frequency analog design software that rises above the rest.

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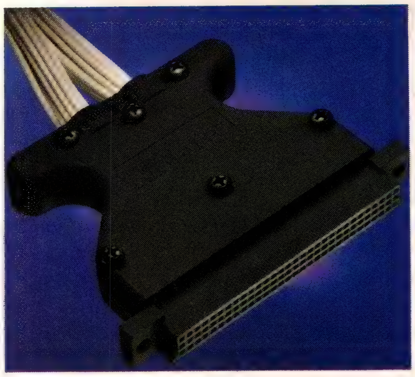
CIRCLE NO. 127

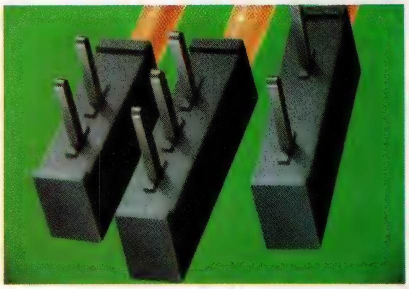
Controlled Impedance Dual Coax Single Signal Interconnects

Meritec controlled impedance Single Signal Interconnect (SSI™) Assemblies are now available in Dual Coax configurations. A common ground may be shared by two subminiature coax cables with separate signals in a 1x3 .100" x 100" format. These coax cables may then be terminated to 1x3s, separate 1x2s, BNCs, SMAs or PCBs. The interconnects are designed to meet the requirements of electrically sensitive applications using high speed CMOS, ECL or GaAs logic. The assemblies are engineered to provide controlled impedance and propagation delay while minimizing crosstalk.



StrainRelief Handles for Meritec Carrier Systems allow frequent removal of the assemblies from the backplane

Meritec has introduced Strain Relief Handles for their Subminiature Coaxial Carrier Systems. The handles provide extra strain relief in applications where the carriers need to be frequently removed from the backplane, i.e. for repairing or rerouting of individual cable lines. The handles feature an interior coax cable management retention system, which consists of two tie-downs that secure cable lines to the inside of the handle. The retention system provides added strain relief and a means of organizing the cable lines into an orderly package.



Low Profile Impedance Matched PCB Solderable Interconnects

Meritec's low profile, impedance matched PCB Solderable Interconnects solder directly to the PC Board for a permanent connection. Pin lenghts of .110" and .160" are available for different board thicknesses. The connectors feature precision, high strength molded terminations for reliability in critical applications. Available in 1 x 2 and 1 x 3 configurations, the connectors are side-to-side stackable and feature heights as low as .150" from the PC Board, making them ideal for dense package applications. Meritec PCB Solderable Interconnects can be terminated to a variety of different subminiature cable types.

Digital and analog interconnect systems that maximize board density and budget.

If you need speed and performance in a digital or analog interconnect system but have a limited budget, turn to Meritec. Meritec digital and analog interconnect systems are designed to meet the requirements of electrically sensitive applications using high speed CMOS, ECL or GaAs logic. Our systems are engineered to provide controlled impedance and propagation delay while minimizing crosstalk. You get ship to stock quality, backed up with technical service and applications support. All at a cost that's well in line with tight project budgets.

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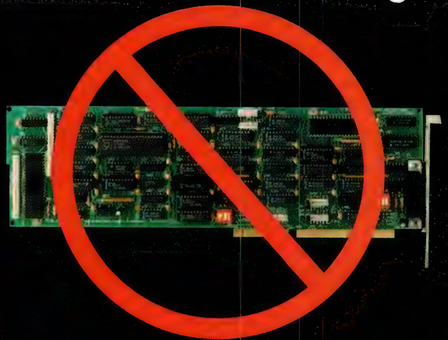
CIRCLE NO. 128

VXI Too Much?

PC Boards Not Enough?



Consider the Data Acquisition Alternatives

Although VXI may be suitable for some test applications, it is overkill for many others. Now, IOtech offers a cost-effective alternative: DAIs, our multi-channel IEEE 488 Data Acquisition Instruments for computer-controlled test systems.

Flexible System Design—Unlike VXI modules, DAIs require no expensive chassis. As a result, a DAI system can cost a fraction of a comparable VXI system. Moreover, because DAIs accommodate the industry-standard IEEE 488 bus, they offer you unequalled system-design flexibility: a DAI system can be augmented with any of the thousands of IEEE products on the market.

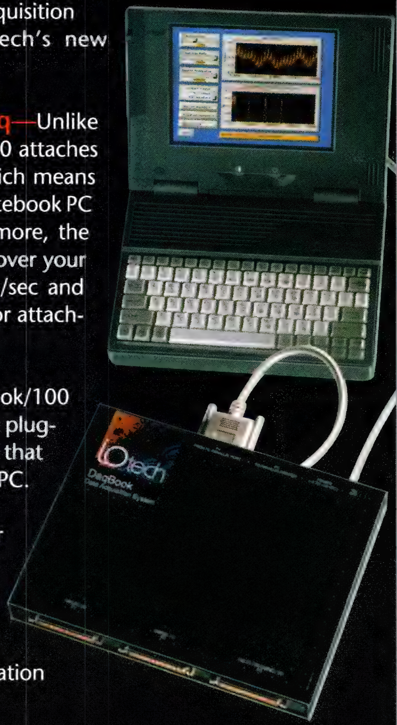
Software Support—Software options for DAI systems include DOS, Windows, and UNIX drivers and support from popular third-party software packages such as Labtech™ Notebook®, HTBasic™, LabWindows®, and LabView®.

If you're considering PC data acquisition plug-in boards, consider IOtech's new DaqBook/100 alternative.

Notebook-based Data Acq—Unlike plug-in boards, the DaqBook/100 attaches to PCs via the parallel port—which means that it works as well with your notebook PC as with your desktop. What's more, the DaqBook/100 can transfer data over your PC's parallel port at 170 Kbytes/sec and includes a second parallel port for attaching your printer.

Small & Versatile—The DaqBook/100 combines the functions of several plug-in boards in one rugged package that fits under the average notebook PC.

Portable—Powered by 12V car battery, rechargeable nickel cadmium battery, or AC line, the compact DaqBook/100 is truly portable, letting you locate your test system wherever your application requires.



For immediate response, call (216) 439-4091.

Data Acquisition Instruments

- *ADC488/16* — 16-ch, 16-bit, 100 kHz A/D
- *Mux488/64* — 64- to 1024-ch multiplexer
- *Mux488/16SC* — 16- to 256-ch thermocouple, RTD, and strain gage multiplexer
- *DAC488HR/4* — 4-ch, 16-bit, 100 kHz D/A
- *DAC488/4* — 4-ch, 12-bit D/A
- *Filter488/8* — 8-ch programmable filter
- *TempScan/1000* — 32- to 992-ch temperature measurement instrument
- *Control488/16* — 16- to 256-ch power controller
- *Digital488HS/32* — 32-ch, 1 Mbyte/s digital I/O interface

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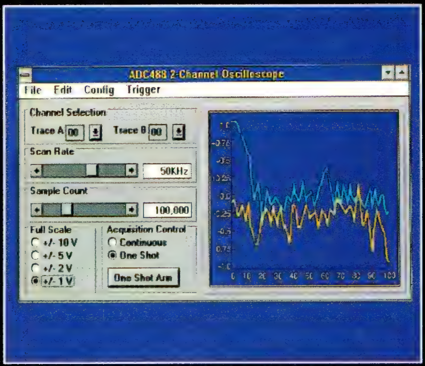

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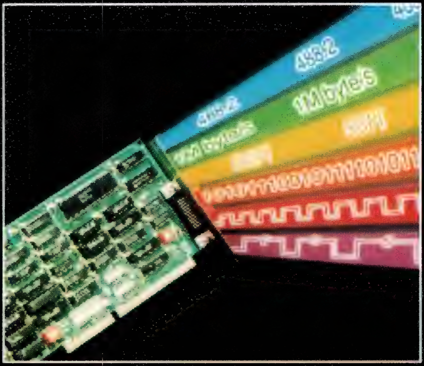

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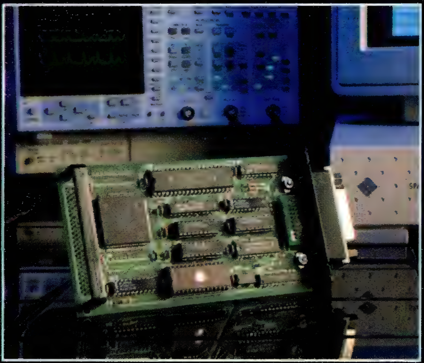

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detector edge-placement error is ±70 psec. Pricing is $10,000 to $13,000 per pin. Delivery is 9 months, ARO. **Advantest America Inc,** 1100 Busch Parkway, Buffalo Grove, IL 60089. Phone (708) 634-2552. **Circle No. 489**

4-port multiplexer for boundary-scan tester. The $495 Mux/4 board allows ProTest systems to simultaneously test four IEEE-1149.1 scan chains in one or more targets. Targets can be scannable ICs or pc boards. The test systems are priced from $7995 to $30,000. **AIS,** 821 Riverside Dr, Los Altos, CA 94024. Phone (415) 941-3247. FAX (415) 941-7642. **Circle No. 490**

SCSI bus analyzer. The 8420 provides 64k frames of capture memory, 20-nsec time-stamp resolution, eight levels of trigger qualification with branch control, and pre- and post-trigger control. The unit provides a nonvolatile memory for setup parameters and includes an RS-232C port that can drive a serial printer to provide hard-copy output. An auto-print feature allows unattended capture of random faults. $2495. **Custom Computer Products Corp,** Box 1137, Hollis, NH 03049. Phone (603) 465-2117. **Circle No. 491**

Macintosh-based token-ring analyzer. Tokenpeek turns a Macintosh on a token ring into a network analyzer that captures all traffic on the ring. The network need not consist only of Macintoshes. The software works with at least 16 protocols; it does require DCA/Avatar Lanway Token-Ring cards, however. The software helps you find performance degradation in its early stages and isolate unproductive rings. $995. **AG Group Inc,** 2540 Camino Diablo, Suite 202, Walnut Creek, CA 94596. Phone (510) 937-7900. **Circle No. 492**

ISA bus isolated analog I/O card. The $399 K16/PC accepts eight inputs that you can program individually for ranges of ±1V, ±100 mV, or 4 to 20 mA. The ADC resolution is 16 bits; the reading speed is 5000 readings/sec; and the error is ±0.02%. Options include a pair of 16-bit DACs, TTL I/O channels, and a floating transducer excitation power supply with 10V and 24V outputs. Dynamic-link library drivers for MS-Windows V3.1 accompany the board. These drivers work with all Windows languages, including VBasic. A virtual-multimeter program also accompanies the board. **Saelig Co,** 1193 Moseley Rd, Victor, NY 14564. Phone (716) 425-3753. **Circle No. 493**

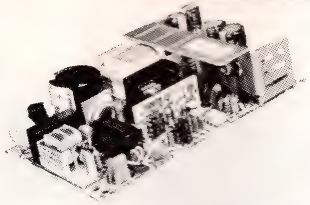
3¾- and 4½-digit DMMs. The $159, 4000-count 390 and the $179, 20,000-count 391 offer respectively 0.1% and 0.05% maximum error on dc voltage measurements. The 390 measures temperature from −50 to 1300°C and capacitance in five ranges to 40 μF. Both models measure frequency—to 500 kHz on the 390; 200 kHz on the 391. Both models also provide an audible continuity indication. The 391 makes true rms ac measurements. **Maxtec International Corp,** 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448. **Circle No. 494**

PID packages for Macintosh and MS-DOS PCs. Versions of this $295 proportional-integral-derivative control software work with two of the vendor's software packages: LabView for the Macintosh and LabWindows for MS-DOS. The algorithms feature bumpless auto/manual transfer, antireset windup, direct/inverse action, and manual output adjustment. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. **Circle No. 495**

Software analyzer. Codeprobe, a companion tool to debuggers and profilers, lets you monitor a program running at full speed, and capture such events as hardware, DOS, and BIOS interrupts, and user-defined events. After an event, you can display a trace in summary or fully decoded form. Time-stamp resolution is under 1 msec and can be as low as 838 nsec if you read registers directly. MS-DOS-based package, $350. **General Software Inc,** Box 2571, Redmond, WA 98073. Phone (206) 391-4285. FAX (206) 557-0736. **Circle No. 496**

Pattern-matching add-on. Genmatch for National Instruments' Labview for Apple Computer's Macintosh systems is

Zenith's ZPS-45



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ZPS-45	45	+ 5.0	0.0/5.0 PK 7.0	+ 12.0	0.0/2.0 PK 3.0	- 12.0	0.0/0.7
ZPS-45-15	45	+ 5.0	0.0/5.0 PK 7.0	+ 15.0	0.0/1.5 PK 2.0	- 15.0	0.0/0.7

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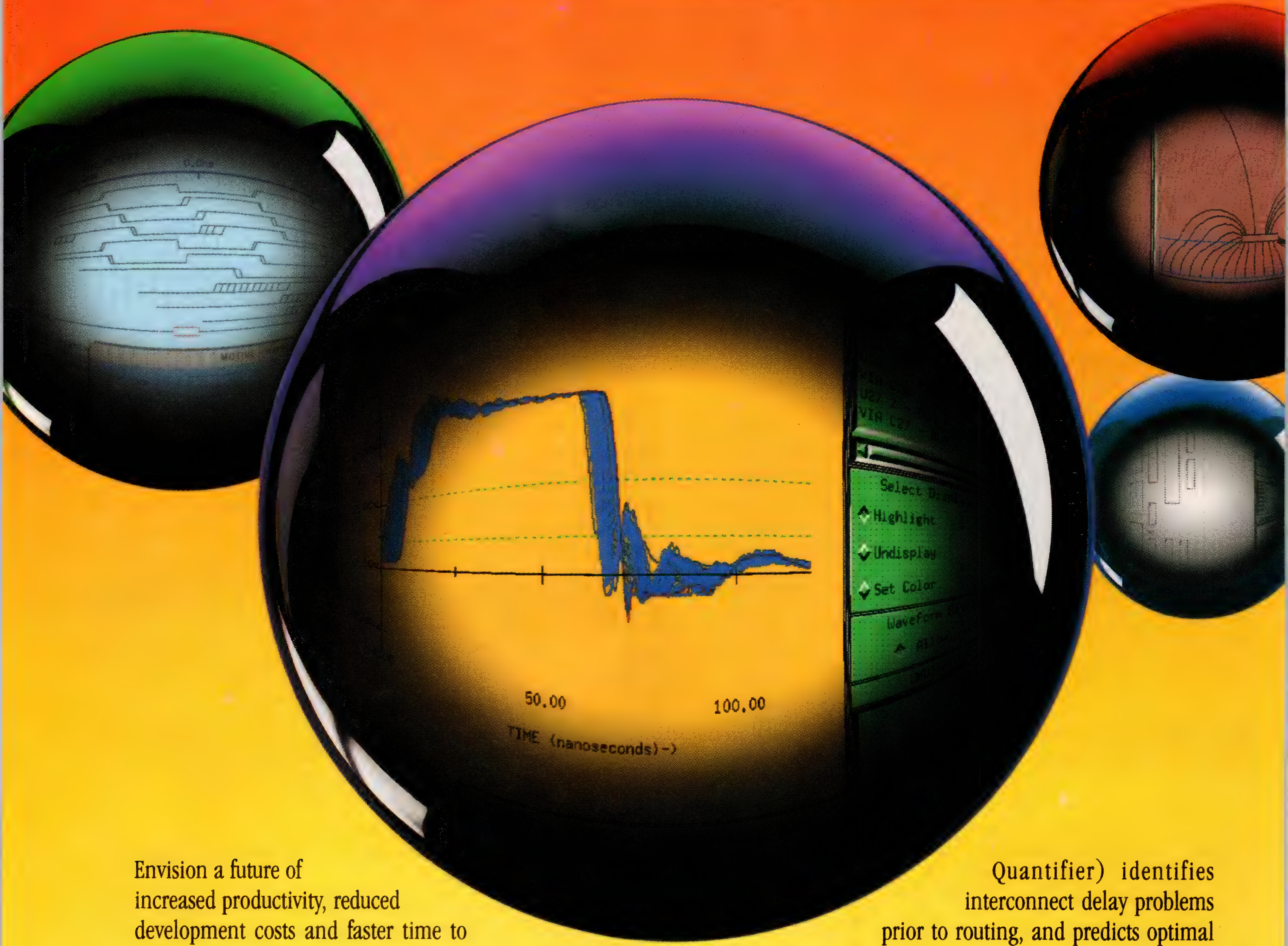

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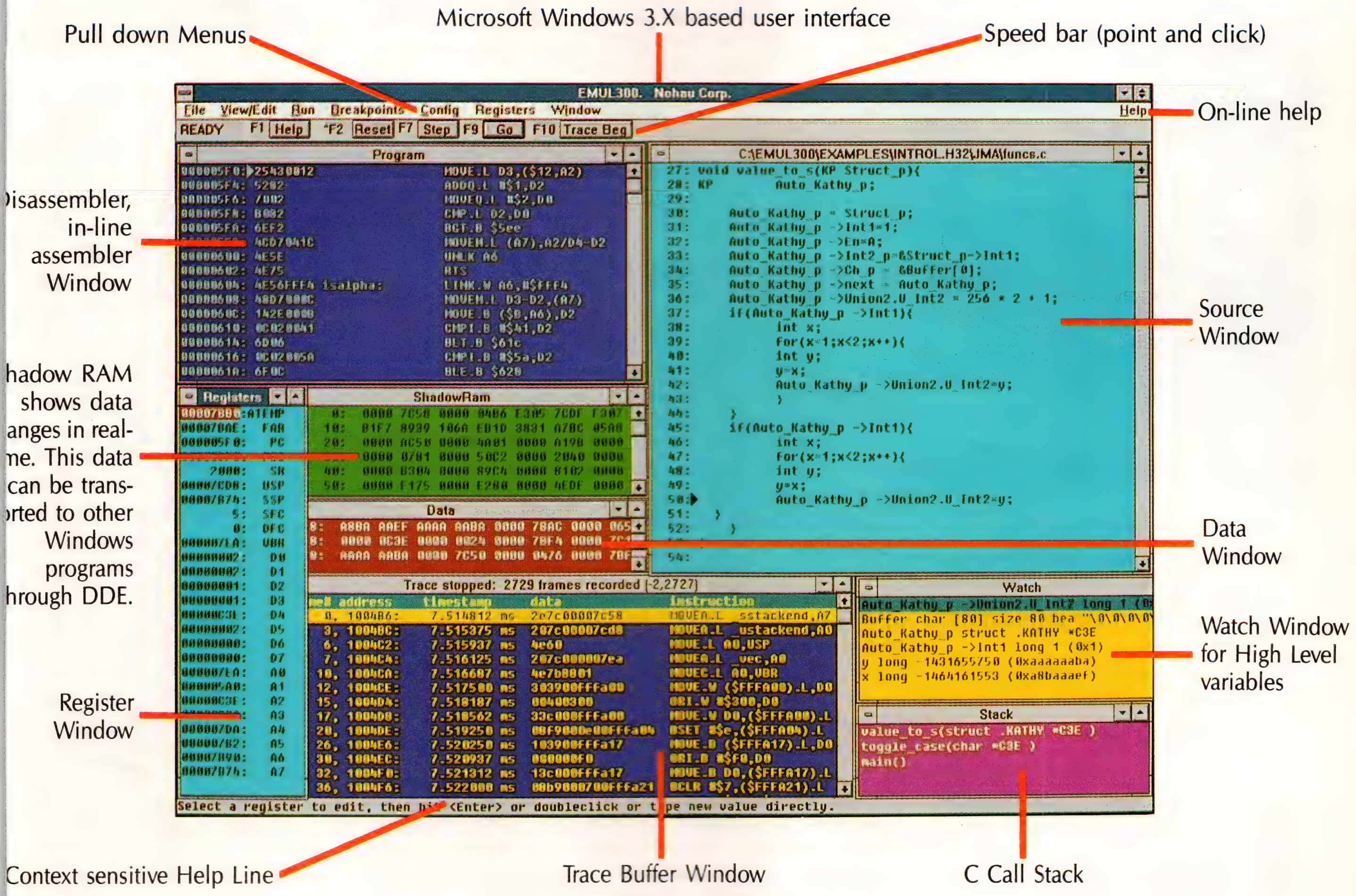
Microsoft Windows 3.X based user interface
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Speed bar (point and click)
On-line help
isassembler, in-line assembler Window
Source Window
hadow RAM shows data anges in real-me. This data can be trans-rted to other Windows programs hrough DDE.
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Watch Window for High Level variables
Register Window
Context sensitive Help Line
Trace Buffer Window
C Call Stack
EMUL300. Nohau Corp.
File
View/Edit
Run
Breakpoints
Config
Registers
Window
Help
READY
F1 Help
^F2 Reset
F7 Step
F9 Go
F10 Trace Beg
Program
Registers
ShadowRam
Data
Watch
Stack

```
000005F0:▶25430012                 MOVE.L D3,($12,A2)
000005F4: 5282                     ADDQ.L #$1,D2
000005F6: 7002                     MOVEQ.L #$2,D0
000005F8: B082                     CMP.L D2,D0
000005FA: 6EF2                     BGT.B $5ee
          4CD7041C                 MOVEM.L (A7),A2/D4-D2
00000600: 4E5E                     UNLK A6
00000602: 4E75                     RTS
00000604: 4E56FFF4 isalpha:        LINK.W A6,#$FFF4
00000608: 48D7000C                 MOVEM.L D3-D2,(A7)
0000060C: 142E0008                 MOVE.B ($8,A6),D2
00000610: 0C020041                 CMPI.B #$41,D2
00000614: 6D06                     BLT.B $61c
00000616: 0C02005A                 CMPI.B #$5a,D2
0000061A: 6F0C                     BLE.B $628
```

```
00007B86:A1EMP
00007BAE:  FAR
000005F0:   PC
[illegible]
    2000:   SR
00007CD8:  USP
00007B74:  SSP
       5:  SFC
       0:  DFC
000007EA:  VBR
00000002:   D0
00000002:   D1
00000001:   D2
00000001:   D3
00000C3E:   D4
00000002:   D5
00000000:   D6
00000000:   D7
000007EA:   A0
000005A0:   A1
00000C3E:   A2
[illegible] A3
000007DA:   A4
000007B2:   A5
00007B90:   A6
00007B74:   A7
```

```
 0:  0000 7C58 0000 0406 E305 7CDF F307
10:  01F7 8939 106A ED1D 3831 A7BC 05A0
20:  0000 AC58 0000 4A01 0000 A198 0000
     0000 0701 0000 50C2 0000 2040 0000
40:  0000 B304 0000 89C4 0000 8102 0000
50:  0000 F175 0000 E280 0000 4EDF 0000
```

```
8:  A8BA AAEF AAAA AABA 0000 78AC 0000 065
8:  0000 0C3E 0000 0024 0000 7BF4 0000
8:  AAAA AABA 0000 7C50 0000 0476 0000 7BF
```

C:\EMUL300\EXAMPLES\INTROL.H32\JMA\funcs.c

```
void value_to_s(KP Struct_p){
KP          Auto_Kathy_p;

    Auto_Kathy_p = Struct_p;
    Auto_Kathy_p ->Int1=1;
    Auto_Kathy_p ->En=A;
    Auto_Kathy_p ->Int2_p=&Struct_p->Int1;
    Auto_Kathy_p ->Ch_p = &Buffer[0];
    Auto_Kathy_p ->next = Auto_Kathy_p;
    Auto_Kathy_p ->Union2.U_Int2 = 256 * 2 + 1;
    if(Auto_Kathy_p ->Int1){
          int x;
          for(x=1;x<2;x++){
          int y;
          y=x;
          Auto_Kathy_p ->Union2.U_Int2=y;
          }
    }
    if(Auto_Kathy_p ->Int1){
          int x;
          for(x=1;x<2;x++){
          int y;
          y=x;
▶         Auto_Kathy_p ->Union2.U_Int2=y;
    }
      }

```

Trace stopped: 2729 frames recorded (-2,2727)

```
ne# address    timestamp     data                instruction
  0, 100486:   7.514812 ms   2e7c00007c58        MOVEA.L  sstackend,A7
  3, 10048C:   7.515375 ms   207c00007cd8        MOVEA.L  _ustackend,A0
  6, 1004C2:   7.515937 ms   4e60                MOVE.L A0,USP
  7, 1004C4:   7.516125 ms   207c000007ea        MOVEA.L  _vec,A0
 10, 1004CA:   7.516687 ms   4e7b0801            MOVEC.L A0,VBR
 12, 1004CE:   7.517500 ms   303900FFFa00        MOVE.W ($FFFA00).L,D0
 15, 1004D4:   7.518187 ms   00400300            ORI.W #$300,D0
 17, 1004D8:   7.518562 ms   33c000FFFa00        MOVE.W D0,($FFFA00).L
 20, 1004DE:   7.519250 ms   08F9000e00FFFa04    BSET #$e,($FFFA04).L
 26, 1004E6:   7.520250 ms   103900FFFa17        MOVE.B ($FFFA17).L,D0
 30, 1004EC:   7.520937 ms   000000F0            ORI.B #$F0,D0
 32, 1004F0:   7.521312 ms   13c000FFFa17        MOVE.B D0,($FFFA17).L
 36, 1004F6:   7.522000 ms   08b9000700FFFa21    BCLR #$7,($FFFA21).L
```

```
Auto_Kathy_p ->Union2.U_Int2 long 1 (0x
Buffer char [80] size 80 bea "\0\0\0\0
Auto_Kathy_p struct .KATHY *C3E
Auto_Kathy_p ->Int1 long 1 (0x1)
y long -1431655750 (0xaaaaaaba)
x long -1464161553 (0xa8baaaef)
```

```
value_to_s(struct .KATHY *C3E )
toggle_case(char *C3E )
main()
```

```
Select a register to edit, then hit <Enter> or doubleclick or type new value directly.
```

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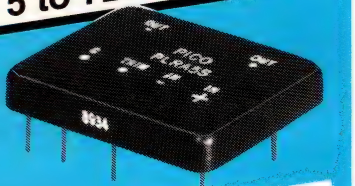

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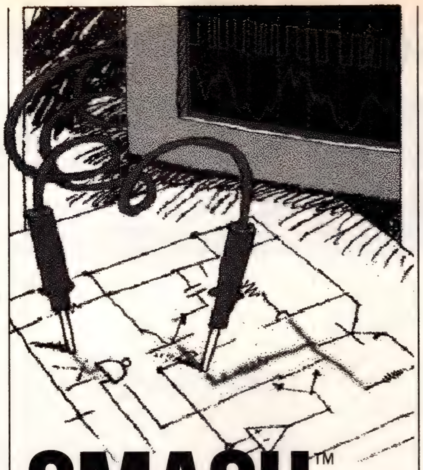

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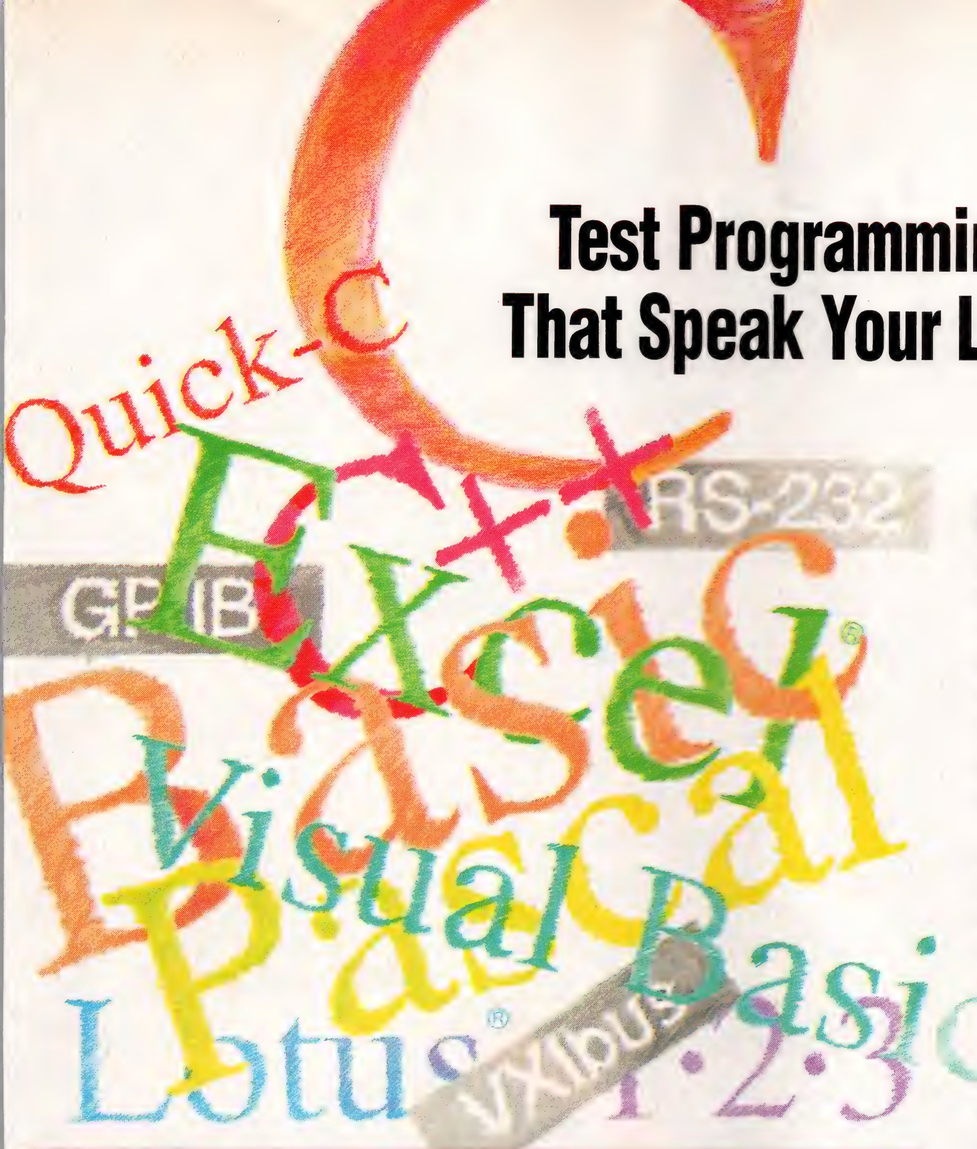

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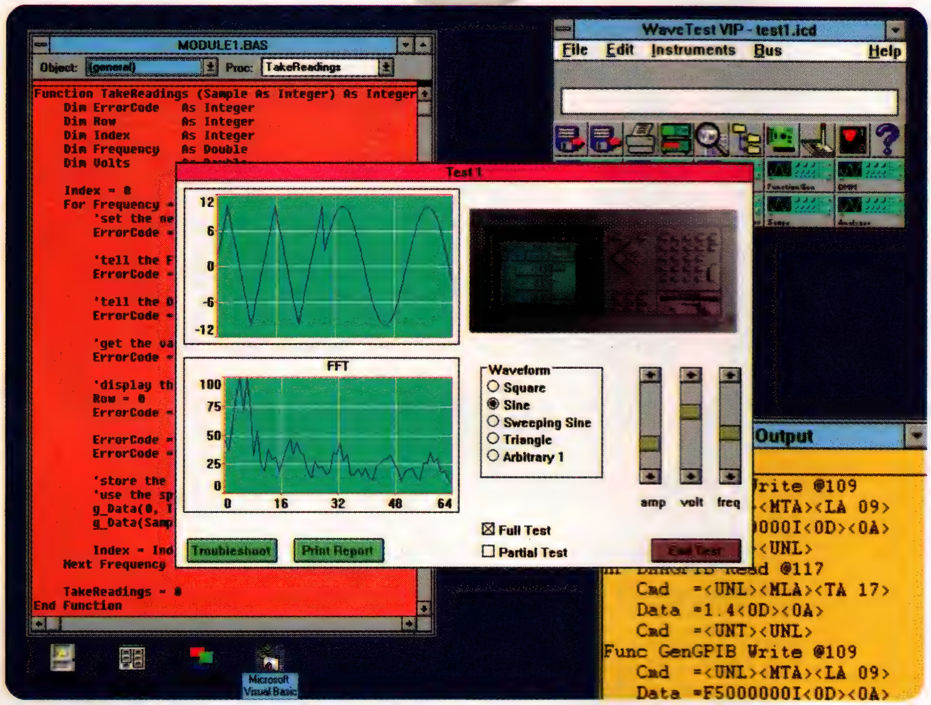

```
Function TakeReadings (Sample As Integer) As Integer
    Dim ErrorCode    As Integer
    Dim Row          As Integer
    Dim Index        As Integer
    Dim Frequency    As Double
    Dim Volts

    Index = 0
    For Frequency =
        'set the ne
        ErrorCode =

        'tell the F
        ErrorCode =

        'tell the D
        ErrorCode =

        'get the va
        ErrorCode =

        'display th
        Row = 0
        ErrorCode =

        ErrorCode =
        ErrorCode =

        'store the
        'use the sp
        g_Data(0, I
        g_Data(Samp

        Index = Ind
    Next Frequency

    TakeReadings = 0
End Function
```

```
rite @109
<MTA><LA 09>
0000I<0D><0A>
<UNL>
    Read @117
    Cmd  =<UNL><MLA><TA 17>
    Data =1.4<0D><0A>
    Cmd  =<UNT><UNL>
Func GenGPIB Write @109
    Cmd  =<UNL><MTA><LA 09>
    Data =F5000000I<0D><0A>
```

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SRS offers a full line of precision electronic test and measurement equipment targeted for both R&D and production applications. SRS products have the features you want, the accuracy you need, the quality you demand, and the low prices which make them truly exceptional values.

Synthesized Function Generators

- 3, 15 or 30 MHz range, all with 1 µHz resolution
- Sine, square, ramp, triangle, and arb waveforms
- Logarithmic / linear sweeps and modulation
- Optional GPIB, RS-232 interfaces

DS335 .... $995
DS340 .... $1595
DS345 .... $2195

FFT Spectrum Analyzers

- 476 µHz to 100 kHz frequency range
- 90 dB dynamic range
- PSD, octave, THD, band, sideband analysis
- Internal source, network analysis (SR770)
- GPIB, RS-232, printer interfaces, 3.5" DOS drive

SR760 .... $4750
SR770 .... $6500

Time Interval / Frequency Counter

- 25 ps single shot resolution
- 1.3 GHz max. frequency, 11 digit resolution
- Statistics, Allan variance, histogram outputs
- GPIB, RS-232 and printer interfaces

SR620 .... $4500

Pulse / Digital Delay Generator

- 4 delay channels, delays to 1000 seconds
- 5 ps delay resolution with 50 ps rms jitter
- GPIB interface, internal or external timebases

DG535 .... $3500

10 MHz Frequency Standard (LORAN-C)

- Cesium clock long term stability (10^{-12})
- Four 10 MHz outputs, adjustable TTL output
- Phase comparator with strip chart output
- GPIB interface, 8' antenna, 100' coax cable

FS700 .... $4950

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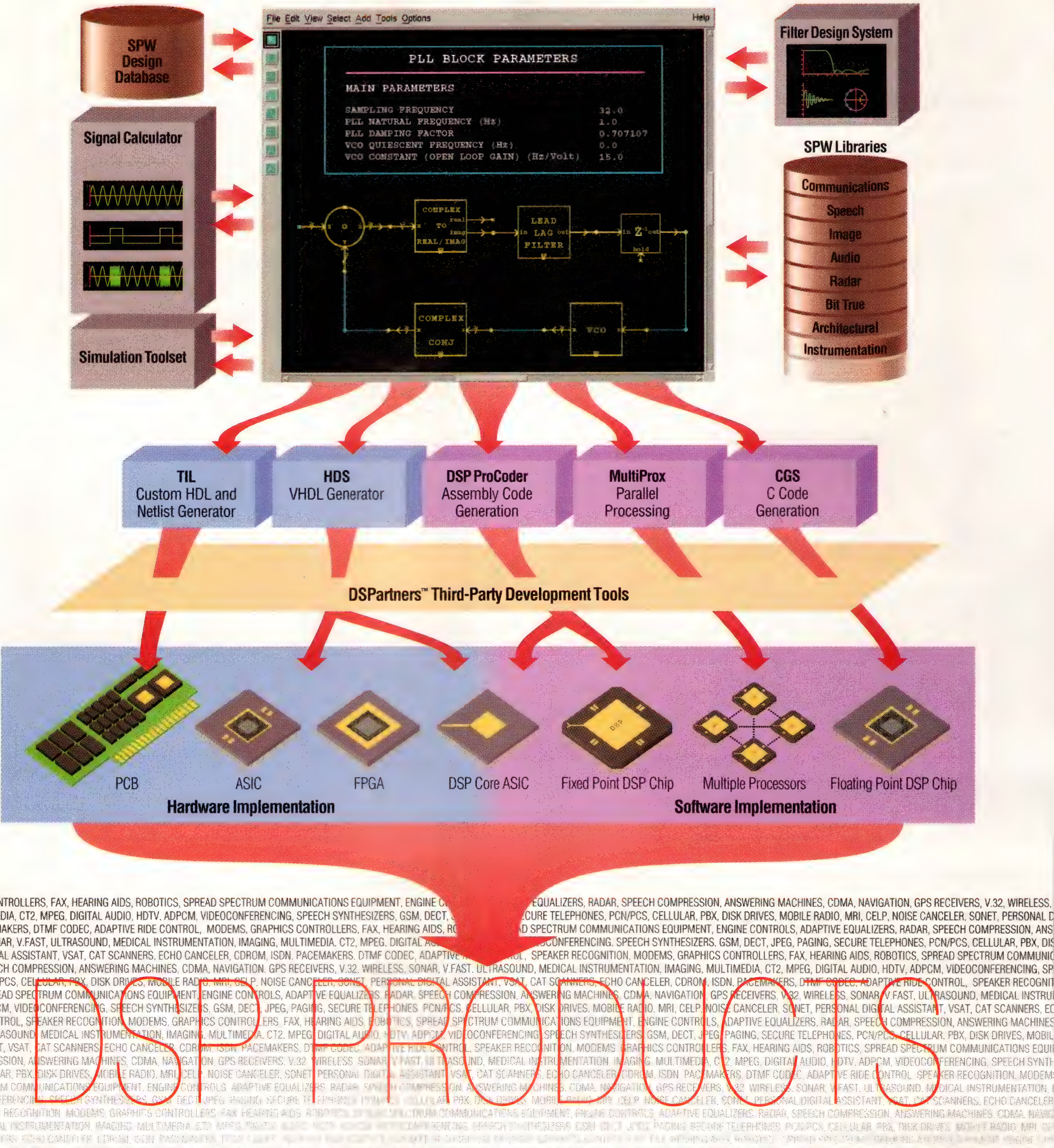

PLL BLOCK PARAMETERS

MAIN PARAMETERS

SAMPLING FREQUENCY	32.0
PLL NATURAL FREQUENCY (Hz)	1.0
PLL DAMPING FACTOR	0.707107
VCO QUIESCENT FREQUENCY (Hz)	0.0
VCO CONSTANT (OPEN LOOP GAIN) (Hz/Volt)	15.0

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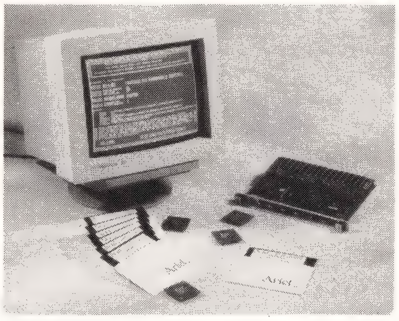
CIRCLE NO. 135

CAE & Software Development Tools



Math libraries for TMS320C40. Pythagoras is a library of routines for performing vector math, signal processing, and image processing on the TMS320C40 DSP chip. The routines were hand coded in TMS320C40 assembly language, and the supplier claims that functions called from C run from 2 to 10 times faster than routines in competitive products. The routines run on any 320C40-based DSP product, including the supplier's own VMEbus-based Hydra and Cyclops DSP boards. You can use the routines to develop software on PCs and Sun workstations. PC version, $1296; Sun version, $1495. **Ariel Corp,** 433 River Rd, Highland Park, NJ 08904. Phone (908) 249-2900. FAX (908) 249-2123. **Circle No. 408**

Signal integrity tool for PC. The DX Series timing-analysis and transmission-line-integrity tools, which run on Quad Design workstations, include a multitasking user interface based on Quarterdeck Office Systems' DESQview/X, thus giving the function and appearance of the OSF Motif GUI running on an X-Window system. The tools include Motive-DX, a fast system-level timing verifier; TLC-DX, which simulates transmission-line effects; XTK-DX, which predicts the effects of signal distortions and ground bounce on circuit performance; and PDQ-DX, which lets you investigate the signal delays. Motive-DX, $16,250; TLC-DX, $10,900; XTK-DX, $19,000; and PDQ-DX, $4750; Unbundled, basic versions also available: Motive-SO, $9950; TLC-SO, $8900. **Quad Design Technology Inc,** 1385 Del Norte Rd, Camarillo, CA 93010. Phone (805) 988-8250. FAX (508) 988-8259. **Circle No. 409**

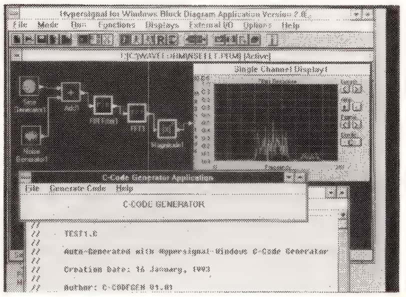
pSOS for SNMP. The SNMP support package provides an industry-standard mechanism to monitor and manage any networked-pSOSystem embedded application from remote computers running SNMP-compatible management software. The basic package includes a target-resident SNMP software library and host computer-based Management Information Base (MIB and MIB II standards) compiler. The compiler lets you write descriptions of target-system characteristics that are readable by computers running SNMP management software. Host systems are Sun SPARCstations and PCs; target systems are the Motorola 68000 family and the Intel i960. From $1400. **Integrated Systems Inc,** 3260 Jay St, Santa Clara, CA 95054. Phone (408) 980-1500. FAX (408) 980-0400. **Circle No. 410**

Programmable-logic design tools. MAX+Plus II Version 3.0 supports Altera's new static RAM-based FLEX 8000 PLDs, plus Altera's MAX 7000, MAX 5000, and Classic families. This new version is available on HP 9000 Series 700 workstations, Sun SPARCstations, and 386- and 486-based PCs. You can use schematic capture, high-level text descriptions, waveform-design entry, or a combination. The tools compile the source files into any of Altera's four programmable-logic families, and you can experiment to find the family that best suits your requirements. $795 to $9995, depending on device and workstation. **Altera Corp,** 2610 Orchard Pkwy, San Jose, CA 95134. Phone (408) 894-7000. **Circle No. 411**

32-bit pc-board layout tools. Printed Circuit Board Layout Tools 386+ incorporate a 32-bit database that gives you unlimited board capacity and high-speed loading. High-speed graphics drivers let you pan and zoom with no delay in redrawing a screen for even the densest boards. The tools automatically generate surface-mount and through-hole footprints from dimensional specs; they create any type of simple or complex pad stack and edit all objects, text, outlines, routes, vias, pads, and holes. $2495. **OrCAD Inc,** 3175 NW Aloclek Dr, Hillsboro, OR 97124. Phone (503) 690-9881. FAX (503) 690-9891. **Circle No. 412**

Windows image-analysis tools. Mocha, an image-analysis system for Windows 3.1, features integrated image processing and measurement, image-annotation tools, a scientific-data worksheet with transform language, and data plotting. It doesn't require a frame grabber to process and measure stored images; you can acquire images from instruments, scanners, and off-site systems and then use your own PC for image analysis. Mocha runs with single or dual monitors. $3995. **Jandel Scientific,** 2591 Kerner Blvd, San Rafael, CA 94901. Phone (800) 874-1888, (415) 453-6700. **Circle No. 413**

Boot-time configuration utility. Bootcon 2.0 lets you create as many as 100 different system configurations and choose any one of them at boot-up time. You no longer have to bother with multiple AUTOEXEC.BAT and CONFIG.SYS files. This new version is compatible with Microsoft MS-DOS 6.0 and supports a mouse. $79. **Modular Software Systems,** 25825 104th Ave SE, Suite 208, Kent, WA 98031. Phone (800) 438-3930, (206) 631-5781. FAX (206) 631-5779. **Circle No. 414**


Hypersignal for Windows Block Diagram Application Version 2.0
File Mode DSP Functions Displays External I/O Options Help
Single Channel Display
C-Code Generator Application
File Generate Code Help
C-CODE GENERATOR

```
//
//    TEST1.C
//
//    Auto-Generated with Hypersignal-Windows C-Code Generator
//
//    Creation Date: 16 January, 1993
//
//    Author: C-CODGEN 01.01
```

Block-diagram DSP tool. Hypersignal-Windows Block Diagram Code Generator adds C-code generation to Hypersignal-Windows Block Diagram, an object-oriented simulation program for signal processing. The code-generation capability lets you move DSP programs from the simulator, where you develop them, to other targets. You need both the new code generator and the original block-diagram tool. Code generator, $2995; main tool, $1995. **Hyperception Inc,** 9550 Skillman, LB 125, Dallas, TX 75243. Phone (214) 343-8525. FAX (214) 343-2457. **Circle No. 415**

Board-support tools for Spectra. Board-support packages (BSPs) for Spectra work with a variety of off-the-shelf target boards from various vendors, including Motorola, Pep Modular Computers, Heurikon, and Radstone. Also available is BSPBuilder, a tool for modifying off-the-shelf BSPs or developing new ones. The BSPs and tools comply with the Logio specification, an open interface to the Spectra software backplane. Individual BSPs, $1500; with SCSI support, $3000; BSPBuilder, $4500. **Ready Systems Inc,** 470 Potrero Ave, Box 60217, Sunnyvale, CA 94086. Phone (408) 736-2600. **Circle No. 416**

CAE & Software Development Tools

Viewlogic design tools for Lattice PLDs. The pDS+ Viewlogic design tools support Lattice's pLSI and ispLSI PLD families. They run on 386- and 486-based PCs under Windows 3.0 and let existing users of Viewlogic software move from field-programmable gate arrays to the faster pLSI and ispLSI PLDs. Viewdraw schematic design-entry package, $800; pDS+ Viewlogic Fitter, $2195; Viewsim functional and timing simulator, $2000. **Lattice Semiconductor Corp,** 5510 NE Elam Young Pkwy, Hillsboro, OR 97124. Phone (503) 681-0118. FAX (503) 681-3077.
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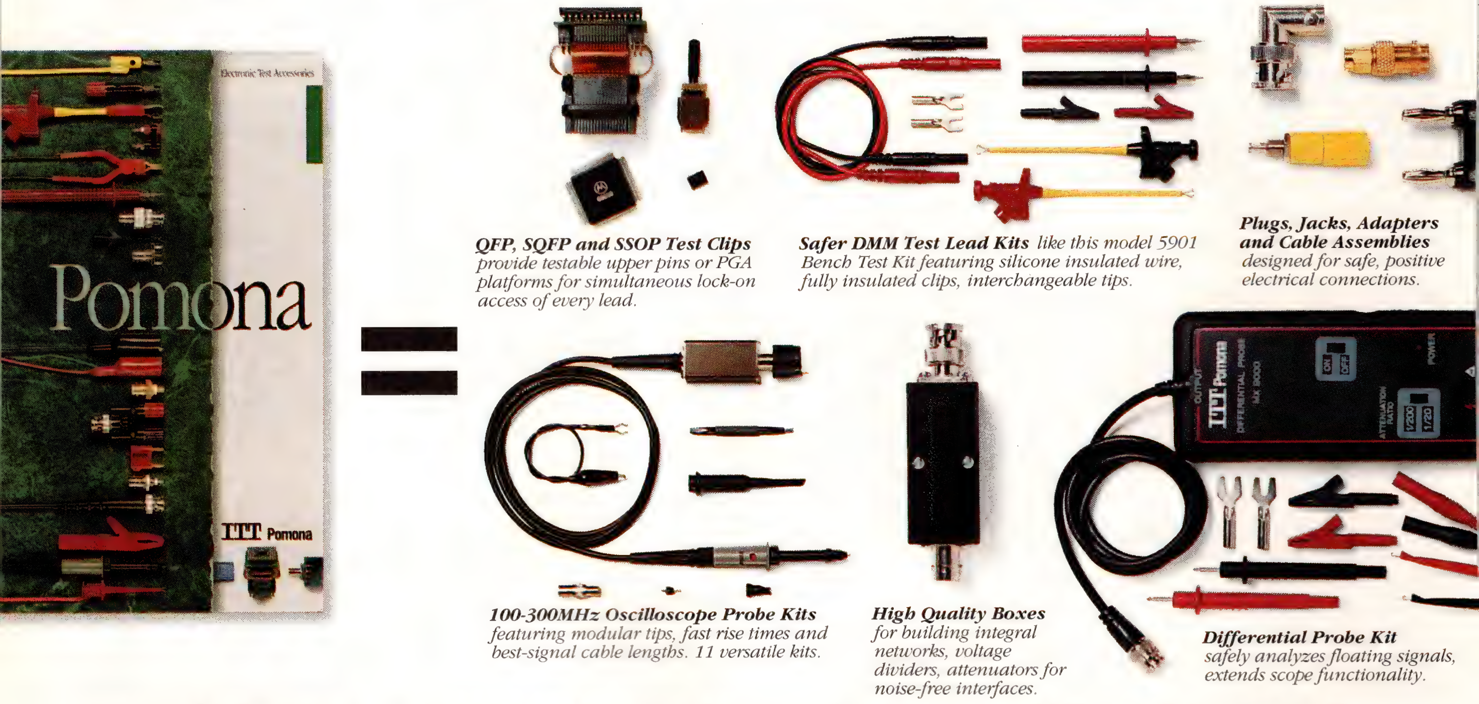
Print Postscript graphics from AutoCAD. CADscript for AutoCAD creates high-quality Postscript presentation graphics for maps, technical illustrations, manuals, overheads, slides, or drawings. The software sends its output directly from AutoCAD drawing files to laser printers, color laser printers, color electrostatic plotters, film recorders, or high-resolution image setters. The product saves you from having to go through a DXF interface to export files to desktop publishing programs. CADscript for AutoCAD works with AutoCAD Release 11 and 12, and it's made by Graphic Computer Services of Australia. $790. **Third Party International,** 6246 SE Scott Dr, Suite 200, Portland OR 97215. Phone (503) 230-8909. FAX (503) 230-9209. **Circle No. 327**
Graphic Computer Services, 2 Second Ave, Mt Lawley, Western Australia 6050. Phone +(619) 370-3234. FAX +(619) 271-8022. **Circle No. 328**

pSOS for VME board. An off-the-shelf board-support package lets you run the pSOS real-time software kernel on the new Motorola MVME162 CPU board. The Motorola board is available (from Motorola) with a choice of processors (68040 or 68LC040) and either with VMEbus support or in "busless" configurations. The board-support package includes pSOS. From $7650. **Integrated Systems Inc,** 3260 Jay St, Santa Clara, CA 95054. Phone (408) 980-1500. FAX (408) 980-0400. **Circle No. 329**

Utility kit for Windows. Winmaster 1.5 includes 40 enhancements over the previous version including optional help bars, adjustable borders, snap-to edges, automatic file launching, and full functioning as a Windows shell and icon browser. This version includes completely rewritten tools for file finding and disk reorganizing. The disk viewer works with additional disk types including CD ROMs, SuperStor volumes, and Microsoft RAM disks. $129.95. **PC-Kwik Corp,** 15100 SW Koll Pkwy, Beaverton, OR 97006. Phone (800) 759-5945; (503) 644-5644. FAX (503) 646-8267.
Circle No. 330

Gate-array physical design library. SLA20000 and SLA20000Plus are libraries for two very low-power, high-performance gate-array families based on a new 0.65-μm N-well double-metal CMOS process. For both libraries the power dissipation is 1.6 μW/gate/MHz with typical gate delays of 0.41 nsec at 3V. The SLA20000 has 545,000 maximum gates (247,000 usable), 592 I/O pads, and level shifters for high-performance and low-power designs using 3 and 5V dual power. The SLA 20000 Plus offers 46,000 maximum gates (25,000 usable) and 208 I/O pads and gives maximum I/O count for low to me-



QFP, SQFP and SSOP Test Clips provide testable upper pins or PGA platforms for simultaneous lock-on access of every lead.

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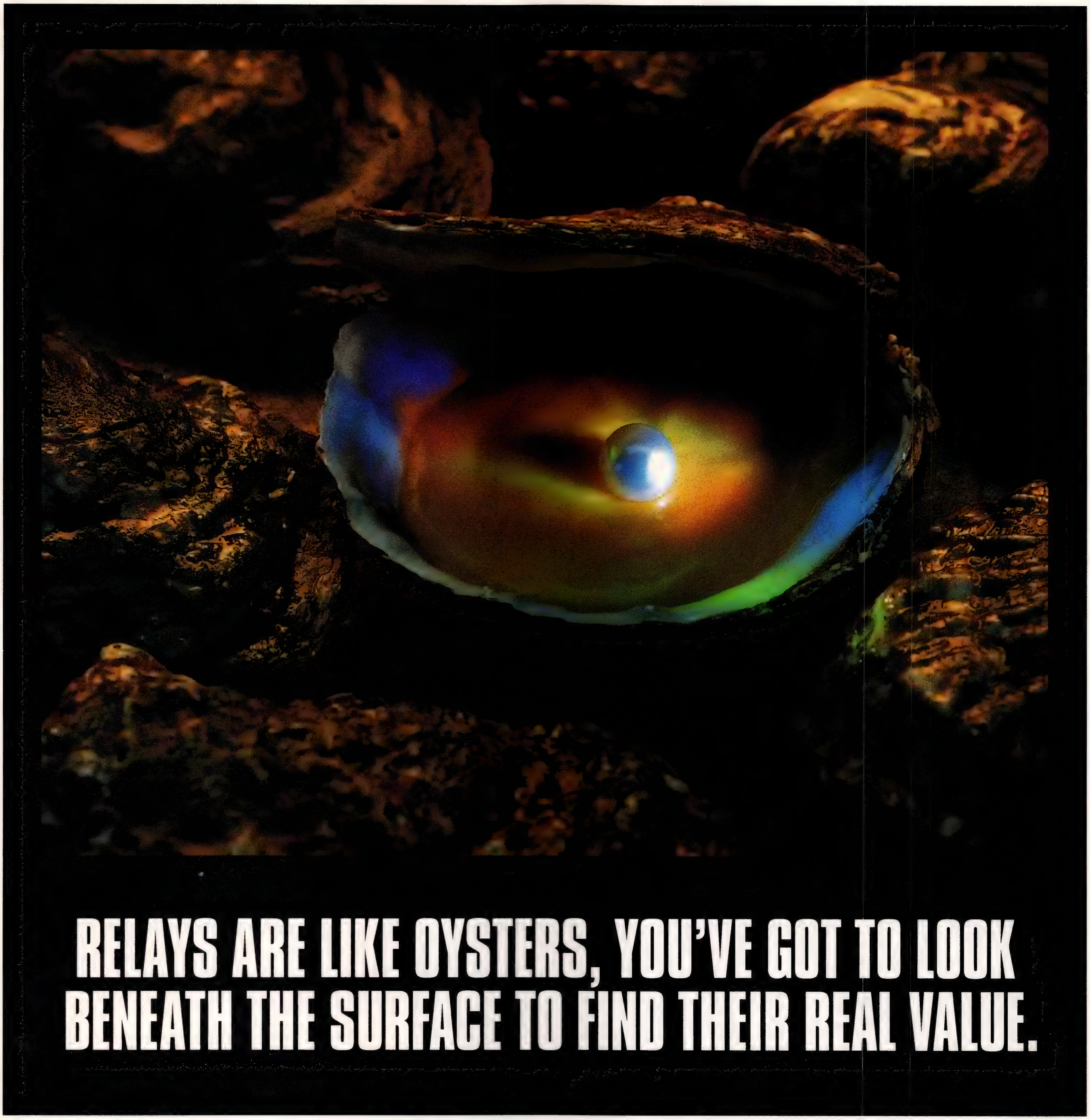
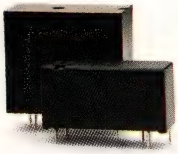

RELAYS ARE LIKE OYSTERS, YOU'VE GOT TO LOOK BENEATH THE SURFACE TO FIND THEIR REAL VALUE.



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dium gate-count designs. Data required for front-end design (schematic capture through simulation) is also available for most major CAE tools. NRE charges for libraries, engineering and CAD services, and prototypes, from $15,000 depending on design requirements. **S-MOS Systems Inc,** 2460 N First St, San Jose, CA 95131. Phone (408) 922-0200. FAX (408) 922-0238. **Circle No. 331**

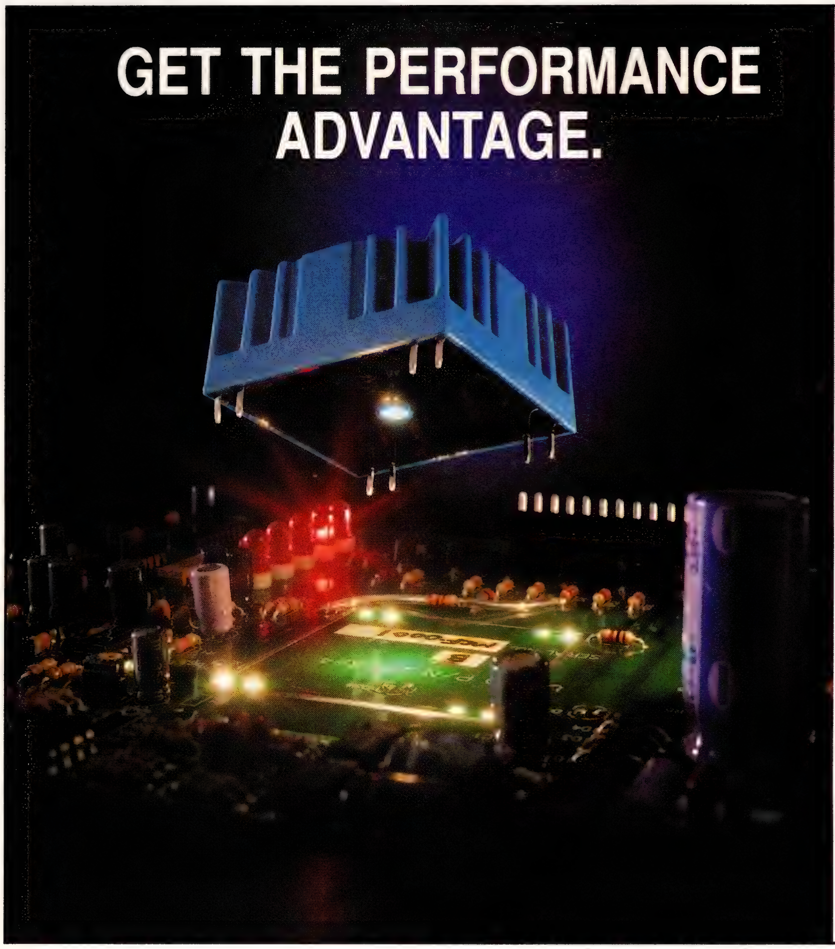
Math tool kit for workstations. Matlab 4.0 combines numeric computation software, a fourth-generation programming language, and application-specific toolboxes. Toolbox types include neural networks, signal processing, control system design and analysis, system identification, and system optimization. For HP Series 700, IBM RS/6000 and Silicon Graphics IRIS Series 4-D workstations, $2995. **The Math Works Inc,** Cochituate Place, 24 Prime Park Way, Natick, MA 01760. Phone (508) 653-1415. FAX (508) 653-2997. **Circle No. 332**

Smith Chart simulation software. ARRL Microsmith 2.00 software simulates a Smith chart. You can use the software even if you don't have a detailed knowledge of Smith charts. This version of the software designs matching networks with fixed or variable LC components, stub-matches sections with transmission lines, makes frequency-dependent terminations, and displays conjugate plots. The software also saves designs-in-progress for quick resuming, and reads Spice files. $39 plus handling. **Amateur Radio Relay League,** Publication Sales, 225 Main St, Newington CT 06111. Phone (203) 666-1541. FAX (203) 665-1166. **Circle No. 333**

Control and data acquisition for PC. The Tele-Graf SCADA DOS software system, which provides functions for real-time data-acquisition and control applications, uses standard protocols via radio, leased line, or telephone dial-up. The system is LAN-compatible, allowing one operator workstation and several view stations. Features include scan rates, calculations, control sequencing, data logging, full trending, and alarm. $2995. **Nota Bene Technology Inc,** 110650 Village Rd, Chaska, MN 55318. Phone (612) 368-4925. FAX (612) 368-3495. **Circle No. 334**

Microcontroller development tool. The PICstart tool family helps you evaluate Microchip's PIC family of 8-bit one-time-programmable RISC microcontrollers and develop code for them. The first member of the family is PICstart-16A, which supports the low-end PIC16C5X group of products. PICstart-16A includes an assembler, a simulator, a programmer board, and chip samples. The tool set runs on PCs. $159. **Microchip Technology Inc,** 2355 W Chandler Blvd, Chandler, AZ 85224. Phone (602) 786-7200. FAX (602) 899-9210. **Circle No. 335**

Visual Basic programming tools. VBAssist 2.0, an extension of Visual Basic, lets you visually create, edit, and save customized versions of objects in the Visual Basic Toolbox. It also lets you create scrollable forms and picture boxes and organize source code with an integrated code librarian. The package can generate dialog and menus from any Visual Basic form for use with SDK-compatible languages. $179. **Sheridan Software Systems,** 65 Maxess Rd, Melville, NY 11747. Phone (516) 753-0985. FAX (516) 753-3661. **Circle No. 336**



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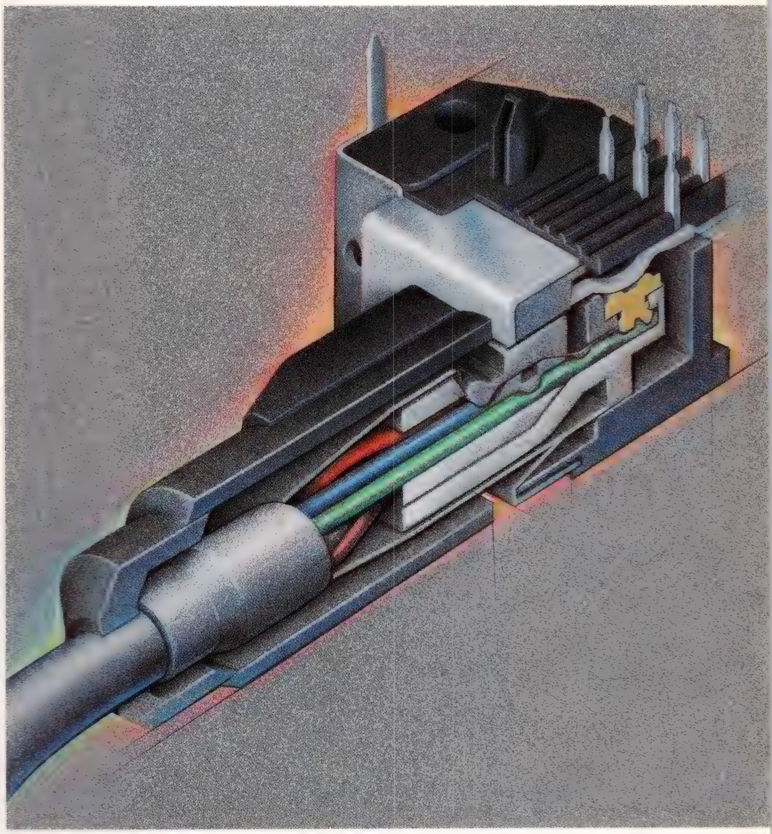

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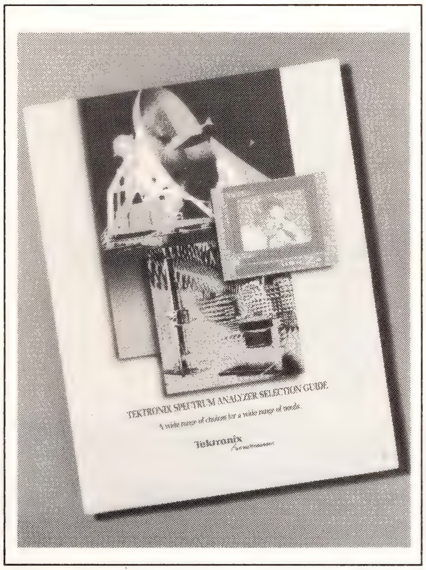
TEKTRONIX SPECTRUM ANALYZER SELECTION GUIDE
A wide range of choices for a wide range of needs.
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Guide for selecting spectrum analyzers. This guide covers a variety of spectrum analyzers for research, design, equipment maintenance, or product test. The guide provides specifications and applications. A "Spec at a Glance" reference chart helps you select the analyzer you need. Literature No. 25A-8527-0. **Tektronix Inc,** Beaverton, OR. **Circle No. 417**

Databook on static RAM. *Fast Static RAM BiCMOS, CMOS, and Module Data* has sections on BiCMOS devices, CMOS devices, ASICs, 3.3V products, and fast SRAM modules. It offers two application notes: "The Motorola BurstRAM" and "A Protocol-Specific Memory for Burstable Fast Cache Memory." The publication also has a reference guide to worldwide sales offices and authorized distributors. Document DL156/D. **Motorola Inc,** Phoenix, AZ. **Circle No. 418**

Brochure on software series. The *The No-Compromise, High-Frequency Analog Design System* brochure outlines the Series IV design system, based on the OSF/Motif graphical user interface. The color publication describes the system in 18 points and provides appropriate illustrations. **EEsof,** Westlake Village, CA. **Circle No. 419**

App note on ADC design. The application note, "Designing a 16-Bit Resolution Sigma-Delta A/D Converter with SPW," demonstrates how to use the signal-processing worksystem (SPW) to design and simulate a 16-bit-resolution sigma-delta ADC in wideband digital-audio systems. A number of block diagrams and waveforms, generated by the SPW, document the design and performance of the converter. **Comdisco Systems Inc,** Foster City, CA. **Circle No. 420**

Catalog of ceramic capacitors. This 52-pg catalog (C-20-A) covers disk and high-voltage ceramic capacitors. It provides specifications for temperature-compensating disks, safety-recognized disks, and miniature disks in voltage ratings from 12V dc to kV dc. The publication also details packaging information. **Murata Erie North America,** Smyrna, GA. **Circle No. 421**

Catalog on disk. The PTA Disk provides a program to help you select A/D, D/A, T/H, sampling-A/D, and multichannel products. It lists product specifications; catalog page references; the Standardized Military Drawing (SMD) number; product part numbers; pin-for-pin competitive cross references; and a time/frequency and frequency/time conversion table. **Micro Networks,** Worcester, MA. **Circle No. 422**

Maybe the best $6\frac{1}{2}$ digit DMM is actually a $5\frac{1}{2}$ digit DMM.

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Turn on a Fluke 8842A and you see a clean, simple front panel, ready to use. HP's 34401, on the other hand, powers up in $5\frac{1}{2}$ digit mode and requires as many as 14 keystrokes before arriving at the specified $6\frac{1}{2}$ digit mode. There's no display to tell you where you are in the process. And if you turn it off, your setup is gone.

Then there's interference. Will common or normal mode noise interfere with your measurements? Will input impedence load your circuits? Not with a Fluke 8842A. It beats HP's 34401 hands down.

If isolation is an issue, Fluke's 8842A provides the 1000V dc you need, unlike HP's 34401 which has just 500V dc.

So if you're looking for a tough, dependable tool, look beyond data sheets and footnotes.

[illegible]	[illegible]	[illegible]
Normal Mode Noise Rejection	>98 dB	>70 dB
Common Mode Noise Rejection	>140 dB	140 dB
MTBF	>100,000 Hrs.	Unknown
Stored Set-Ups	Not needed	No
Input Impedance @20V	10,000 MΩ	10 MΩ
dV Ranges	Six: 20 mV -1000V	Five: 100 mV -1000V
Isolation Common Mode Voltage	1000V dc	500V dc
Basic One Year DC Accuracy	±0.003%	±0.0035%

You'll choose the Fluke 8842A. For more information, contact your local Fluke representative. Or give us a call toll-free at **1-800-44-FLUKE** (1-800-443-5853).

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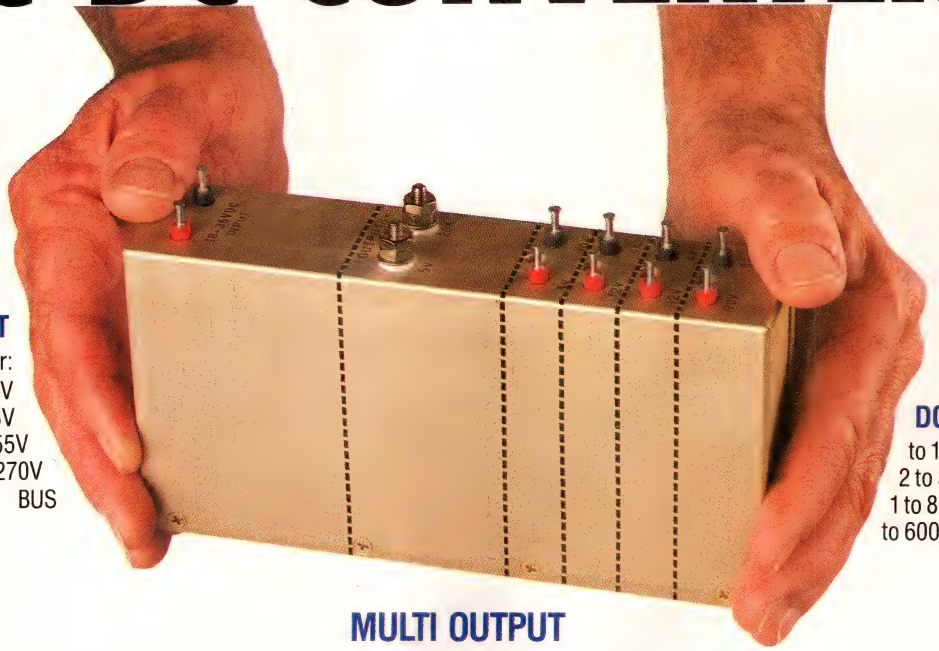

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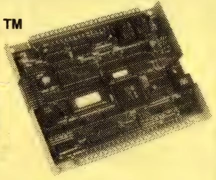

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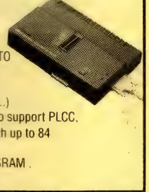

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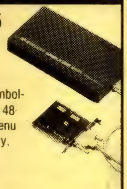

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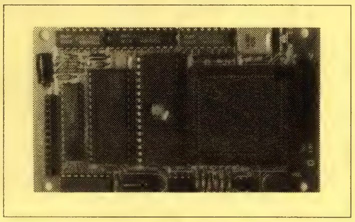

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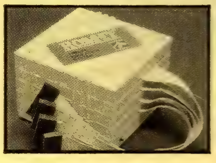

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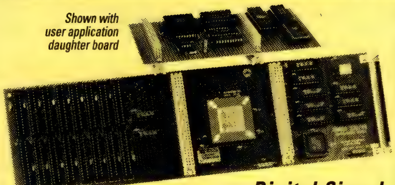

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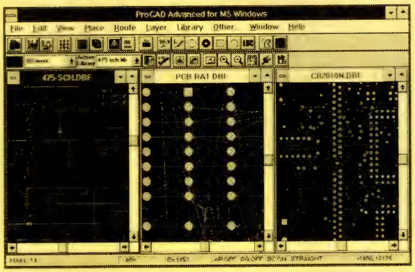
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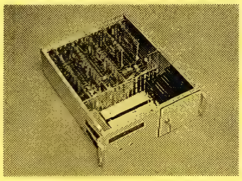

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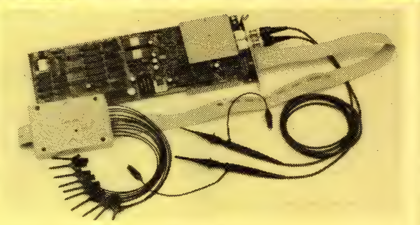

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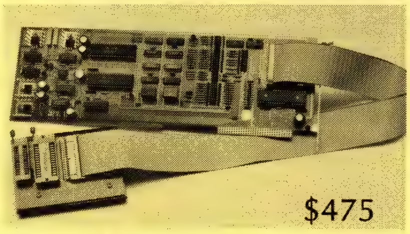

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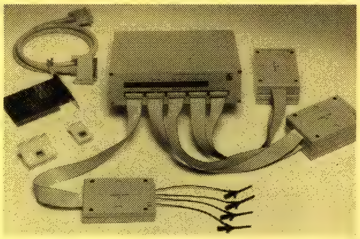

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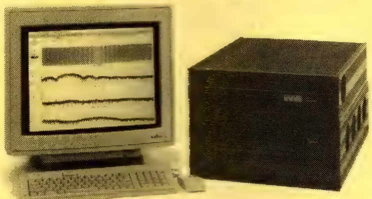

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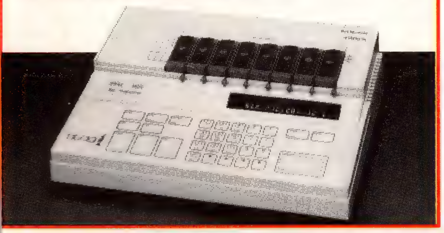

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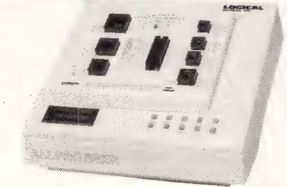

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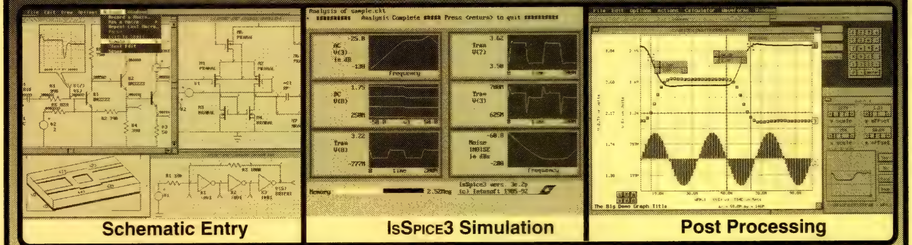

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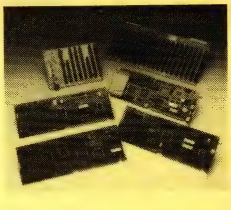

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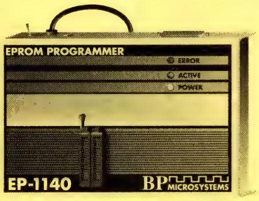

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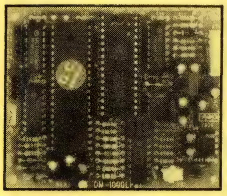

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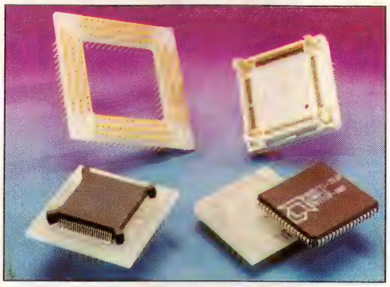

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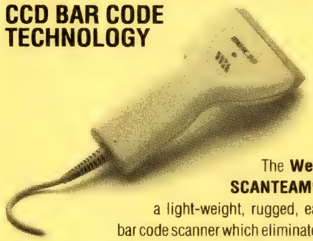

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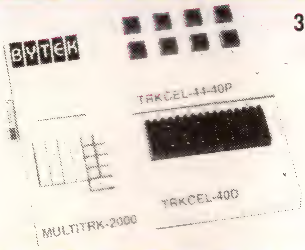

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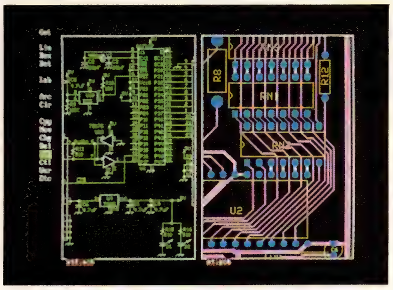

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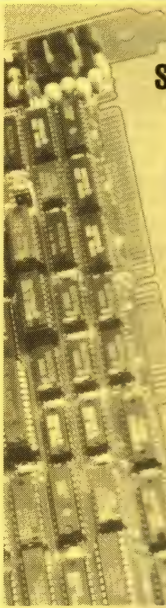

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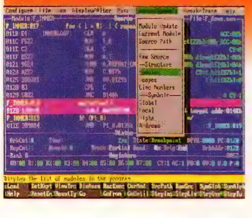

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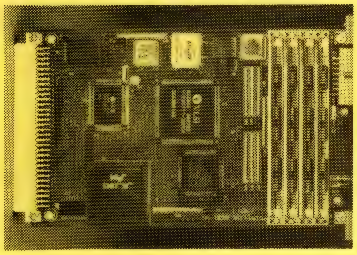

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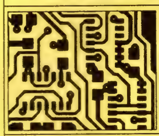

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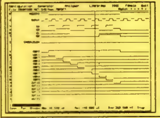

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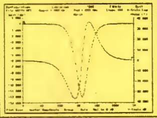

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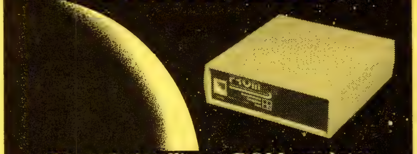

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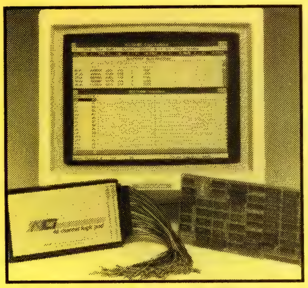

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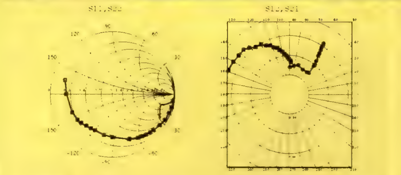

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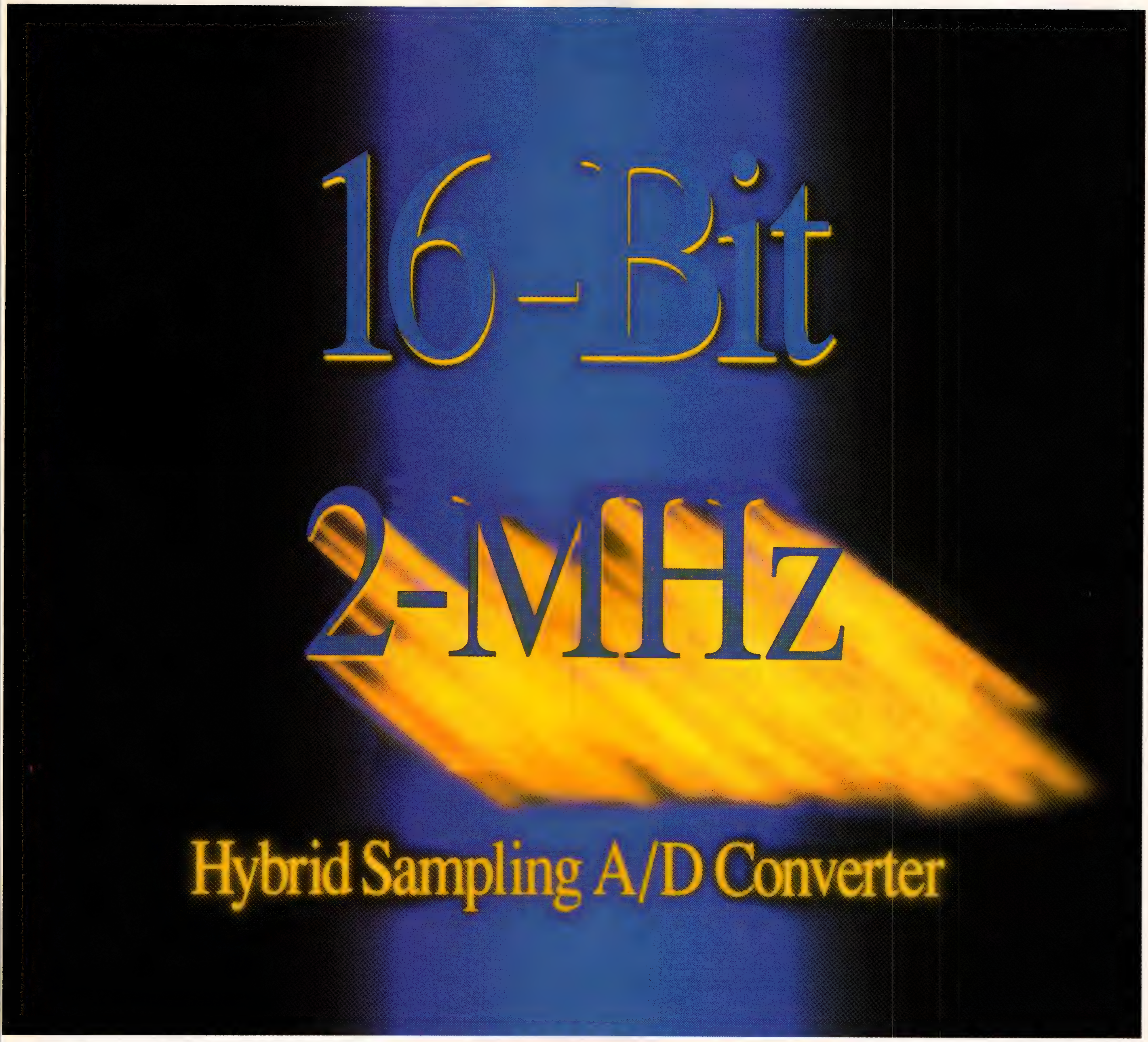

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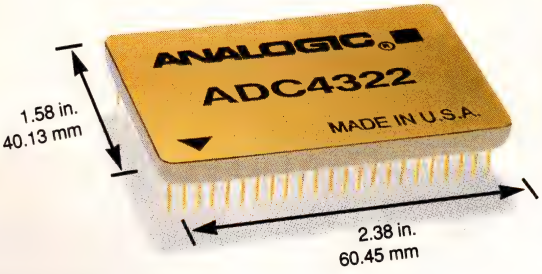

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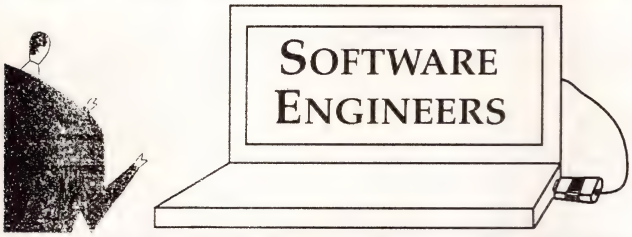

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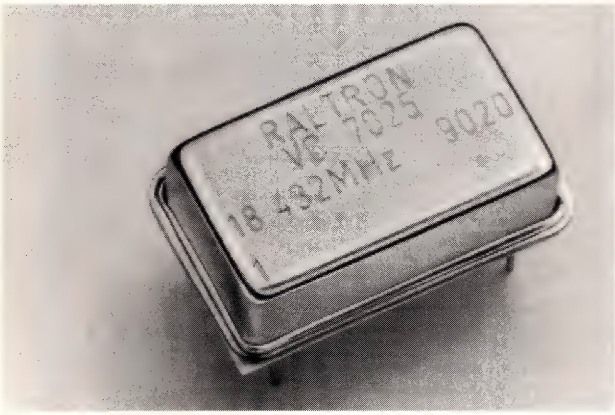

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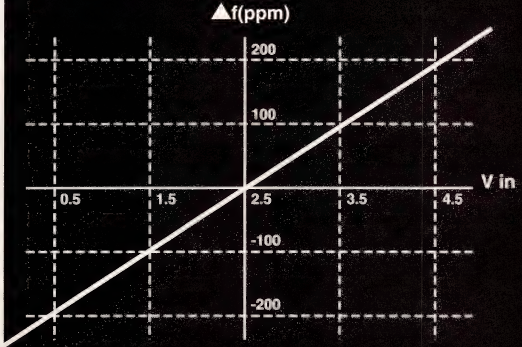

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A good modem is the key to the new and exciting world of electronic-bulletin-board systems (BBSs). And, some advanced, 9600-baud, error-correction, data-compressing modems are available for street prices of less than $300 (try Peripheral Express at (800) 299-0200).

Having had the pleasure of communicating at 9600 baud, I will never, ever go back to 2400 baud. Screens of text appear in a flash. Files that once took half an hour to download now download in minutes. Line noise that used to drive me to distraction never garbles my messages or blows my connection down. Using a 9600-baud modem, BBS communications take place at the speed of thought.

I borrowed advanced modems from ATI Technologies, Digicom Systems, UDS Motorola, and US Robotics. Now don't think that I experimented with a statistically valid number of modems, subjecting them to exhaustive, ANSI-standard tests of all their operating modes using the latest in megabucks test gear. My more modest goal was simply to see how the modems performed, and how easy they were to work with, for the average BBS patron.

I tried the modems out at work and at home, communicating via Datastorm's Procomm—a popular and simple communications program available in commercial and shareware versions. I also cycled the modems through the lab of the maker of our BBS's software, Galactacom. Then I hooked the modems up to the EDN Readers' BBS after getting the all-important "init string" from Galactacom. Further, I enlisted the aid of a "sysop" (system operator) of a Mac conference of a local computer society to get a "Mac-fanatic" data point or two.

The good news is that all of the modems were easy to set up and performed flawlessly under Procomm running on several different IBM PC clones. The Mac fanatic, on the other hand, almost suffered a nervous breakdown getting the modems running. After many frantic phone calls to various bemused, but helpful applications engineers, the Mac fanatic learned to his dismay that his old Mac's RS-232C port has a fundamental hardware deficiency that makes high-speed "modeming" difficult. Nonetheless, once the Mac fanatic got a 9600-baud modem running, he was so pleased with the unit's performance that he did not want to return the evaluation unit. Incidentally, he is also buying a newer Mac.

Galactacom reported that all of the modems worked perfectly at their test site in Florida after being initialized with the proper "init string." Alas, I could not replicate these results. Except for the dead-reliable US Robotics modem, the other 9600-baud modems would occasionally lock up on the EDN Readers' BBS despite using Galactacom's init strings—and a couple of variations of my own, too.

The problem seemed to be that the BBS software sometimes did not understand messages from the modems. Note that 9600-baud, er-

Engineers network with peers electronically via BBSs

BBSs are a unique combination of point-to-point, private communication and worldwide broadcasting that are curiously underutilized by engineers. According to an EDN survey, only a tiny fraction of all engineers who have access to a computer and a modem use BBSs. One reason for not using BBSs could be a reluctance to rack up expensive long-distance phone charges. A 9600-baud modem will cut your BBS phone bills by more than 75%.

Some BBSs, such as the EDN Readers' BBS, allow you to "attach" a file to a private e-mail message or a public-forum message. The combination of a text message and an attached file of computer-readable material uniquely suits the knowledge needs of engineers (by using common file-compression utilities you can compact many files into a single file suitable for attachment). Over a BBS, engineers working in even highly specialized niches can communicate and help each other solve problems.

Now you say that you work for a defense contractor who frowns on engineers' phoning out to computers and discussing their work on public forums. Or, you say you work for a company that forbids foreign software because they fear computer viruses. Even so, you can download material from BBSs at home, print it out, and use the listings as the basis for your own programs. Further, you can always get virus-free copies of shareware directly from the author or from a reputable shareware dealer for only a modest media charge or registration fee.

ror-correcting modems naturally emit a wider variety of control messages than do 2400-baud, dumb modems. However, untended, 24-hour/day operation is only important to BBS sysops, so I didn't consider my BBS problems to be significant for the average user.

Anyone used to the simple handshake sequence of two 2400-baud, Hayes-knockoff modems "syncing" up will be startled the first time he hears a pair of advanced modems go to town. The 2400-baud modems simply exchange two tones and a burst of FSK (frequency-shift keying). The 9600-baud, error-correcting, data-compressing modems take what seems like forever to exchange a startling series of beeps, blips, whoops, and squawks before settling down to a mutually agreed-upon baud rate, correction scheme, and compression scheme.

The reason for the extended handshaking is that both modems have to decide on one of four or five baud rates, one of two error-correcting schemes (each of which has several different "levels"), and one of two data-compression schemes. When it works, it's marvelous. When it doesn't, it's time to hit the modem manuals.

Each manufacturer has its own very definite ideas on how to "extend" the defacto standard Hayes "AT" commands. That is, the basic commands are *more or less* the same (I did say "defacto," didn't I?) but the commands for the advanced features are different from modem to modem. Come to think of it, the mix of advanced features are different, too.

In keeping with a long-standing modem-industry tradition, the manuals tell you what each extended command will do but keep silent on just why anybody would (or would not) want to do that thing. Nor do they usually provide any correlation between users' problems and suggested command changes. I don't know about you, but when I turn to a modem manual I am usually frustrated by my modem's mysterious refusal to communicate, and I just want to know which command or commands to fool with to fix the ding-dang problem I am having.

The other day, I caught myself rattling off a series of Hayes AT commands and S-register changes to an EDN reader who was having trouble logging on to the EDN Readers' BBS. I realized, with horror, that I had the entire Hayes AT command set memorized. Believe me, this is knowledge I fervently wish I had never acquired.

"A good modem is the key to the exciting world of bulletin board systems."

Luckily, IBM PC users don't need to understand an entire modem manual. They can rely mostly on the "default" command settings the modems use to power up—plus just a few of the extended commands. An IBM PC user needs to jot down only the commands for locking the advanced modem at 2400 baud, turning off data compression and turning off error correction. Mac users . . . good luck!

I tried logging on to a variety of BBSs. If the default settings didn't work, I commanded the advanced modem to become a dumb, 2400-baud modem. That always did the trick. You see, some 2400-baud modems, when called, will not wait around for an advanced modem to "fall back" through all of its intermediate modes before the advanced modem decides to be a dumb, 2400-baud modem, too. In other troublesome hookups, the culprit was an older MNP modem. The MNP error-correcting protocol has a reputation for being more annoying and less reliable than the newer V.32 and V.42 protocols. Logging on as a dumb, 2400-baud modem first, and then repeatedly relogging on (enabling a different feature each time) usually got me connected properly to MNP modems—eventually.

Note that for error-correction to work, the baud rate of the connection between your computer and your modem obviously has to be higher than the baud rate of the telephone connection. Having the better grade of UART in your PC—one having an internal buffer—helps, too. In other words, buying the cheapest serial-communications board and Hayes-knockoff 2400-baud modem for your 66-MHz 486-based PC is like putting propellers on a Learjet.—**Charles H Small**

ATI Technologies Inc, 3761 Victoria Park Ave, Scarborough, ON M1W 3S2, Canada. Phone (416) 756-0718. FAX (416) 756-0720. Model 9600ETC.E, $389.

Datastorm Technologies, Box 1471, Colombia, MO 65205. Phone (314) 443-3282.

Digicom Systems, 188 Topaz St, Milpitas, CA 95035. Phone (408) 262-1277. Model 9624LE, $695.

UDS Motorola, 5000 Bradford Dr, Huntsville, AL 35805. Phone (205) 430-8000. Model V.32/5 FasTalk, $695.

US Robotics, 8100 N McCormick Blvd, Skokie, IL 60076. Phone (708) 982-5010. Model Courier V.32, $695.

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Text continued on pg 304

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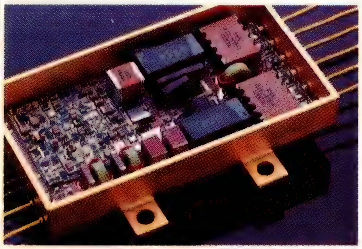

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CIRCLE NO. 145

Software calculates high-frequency winding losses

Finite-element analysis (FEA) software helps you understand the magnetic and electric fields in power converters and their components. As a result of this understanding, you can reduce power losses and component volumes. In the past few years, several software packages that use FEA techniques to calculate power losses directly from the Maxwell equations have emerged. Two such packages are the Maxwell 2D and Maxwell 3D Field Simulators from Ansoft Corp.

These packages avoid the assumptions and approximations that are a practical necessity in the traditional approach of estimating field intensity, but which introduce inaccuracies. In addition to giving values for additional loss, finite element modeling can display the fields and current distributions that are the sources of the losses. You can use this information to optimize core and winding geometry, reducing system size, cost, and power loss. The packages are available on Unix-based workstations and DOS-based PCs.

You don't have to have a specialized knowledge of FEA to get results with the packages, because a menu guides you through the process. The first step is to draw a 3-D model of the device or structure you are analyzing by using a full-featured solid modeler that is included with the program. The system automatically generates and adaptively refines a finite-element mesh. The system then assigns material properties such as permeabilities, conductivities, and permitivities to each object in the model. Excitations include currents, voltages, charges, external fields, and permanent magnets. The system performs all FEA computations internally, so that you can generate the field solution with a single command. The system also automatically computes special quantities of interest such as force, torque, inductance, and capacitance. A post processor lets you display, manipulate, and analyze the field solutions.

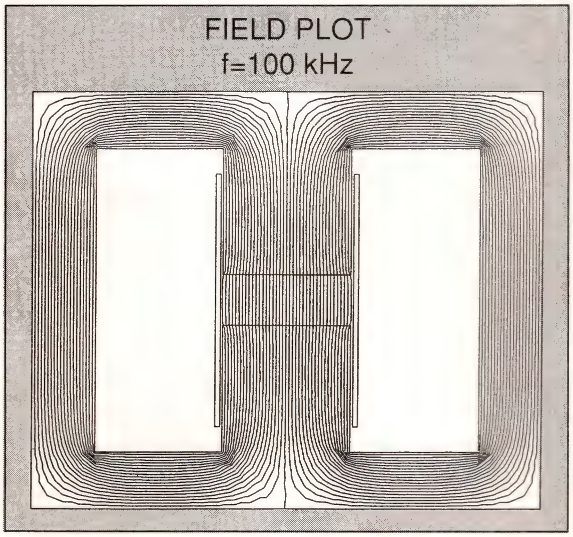

Fig 1—All of the current is concentrated in a thin strip adjacent to the gap in this winding generated by the Maxwell 2D software. The apparent lack of a gap-leakage field is due to cancellation by the large eddy current in the winding.

Figs 1 and **2** illustrate the understanding of magnetic and electric fields that the software gives you. It would seem from the field distribution that there is little or no fringing field due to the gap, thus classical techniques, such as Dowell's analysis (**Ref 1**) would appear to be appropriate. However, a plot of the current density along the inner edge of the winding that the Maxwell 2D package generates shows that essentially all of the current is concentrated in a thin strip adjacent to the gap. The apparent lack of a gap leakage field is due to cancellation by the large eddy current in the winding. At dc, the winding loss for this example would be 26W. At 100 kHz, the winding loss predicted by normal-proximity-effect analysis would be 63W. The power loss for the current distribution shown in **Fig 2** is 345W—5.5 times the loss predicted by the conventional approach.

Having this information available makes it possible to reduce the loss by moving the winding the optimum distance away from the gap. It is desirable to move the winding far enough away to minimize the losses, but not so far as to greatly enlarge the window size. Moving the winding away from the gap by a distance equal to twice the gap reduces the winding loss to 78W, which is only a 24% increase over the ideal. Moving the winding even further away reduces the loss even more, but would probably result in excessive window size. Another alternative would be to use a multiple gap structure, with small air gaps and a reduced winding window.

A full wave-center-tapped rectifier connection that is typical for low-voltage, high-current outputs provides another example. In this circuit, each of the secondaries conducts alternately with a half-wave current in each side. As the frequency and power level are raised, it becomes possible to use a single turn for each of the secondaries. The usual proximity effect calculation would indicate that the optimum layer thickness for each of the windings is in the range of 0.8 to 1.8 skin depths at the frequency of operation, depending on the current waveform.

Such a transformer might be

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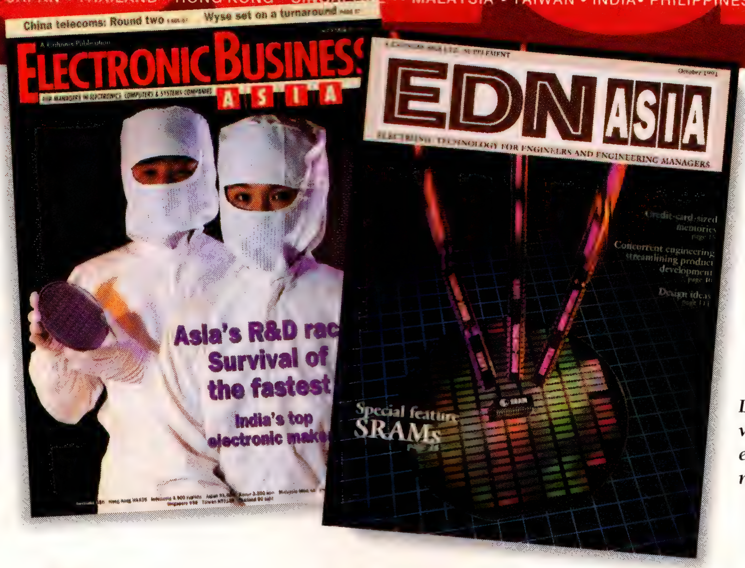
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wound with the low-voltage, high-current secondaries on two outer turns. The two outer turns are the low-voltage, high-current secondaries. From the normal calculation, one would expect a winding loss of about 0.8W, but experience shows that the actual losses are much higher. You can determine the reason for this by plotting the current densities in the windings using Maxwell 2D software when S2 is conducting. The loss in S2 is the expected 0.877W, but the loss in S1 is 0.6W, even though it has no average current flowing in it. The reason for this unexpected dissipation is the eddy current induced in S1 by the current in S2. Two possible ways to reduce or eliminate this problem are to adjust the relative thickness of S1 and S2 to minimize the additional loss, or to use another topology, such as a forward converter or a 2-inductor voltage-divider rectifier. Both approaches let you use a single secondary so that there is no eddy current loss in an inner secondary. You can easily determine the relative advantages and disadvantages for each of these approaches, which depend on the specific application, with finite-element analysis.—**Rudy Severns**

Ansoft Corp, Four Station Square, Suite 660, Pittsburgh, PA 15219. Phone (412) 261-3200. FAX (412) 471-9427.

Author's biography

Rudy Severns is the president of Springtime Enterprises Inc in Cottage Grove, OR. You can reach him at (503) 942-0536.

Reference

1. Dowell, PL, "Effects of Eddy Currents in Transformer Windings," Proceedings of the IEE, Vol 112, No. 8, August 1966, pp 1387 to 1394.

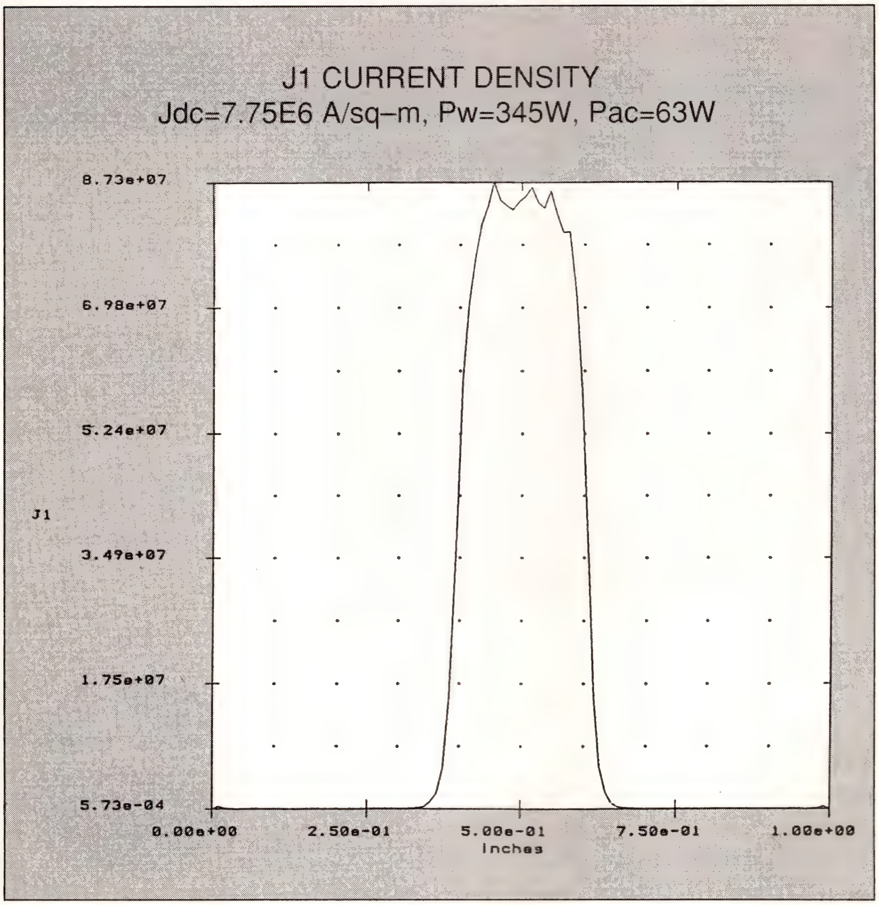


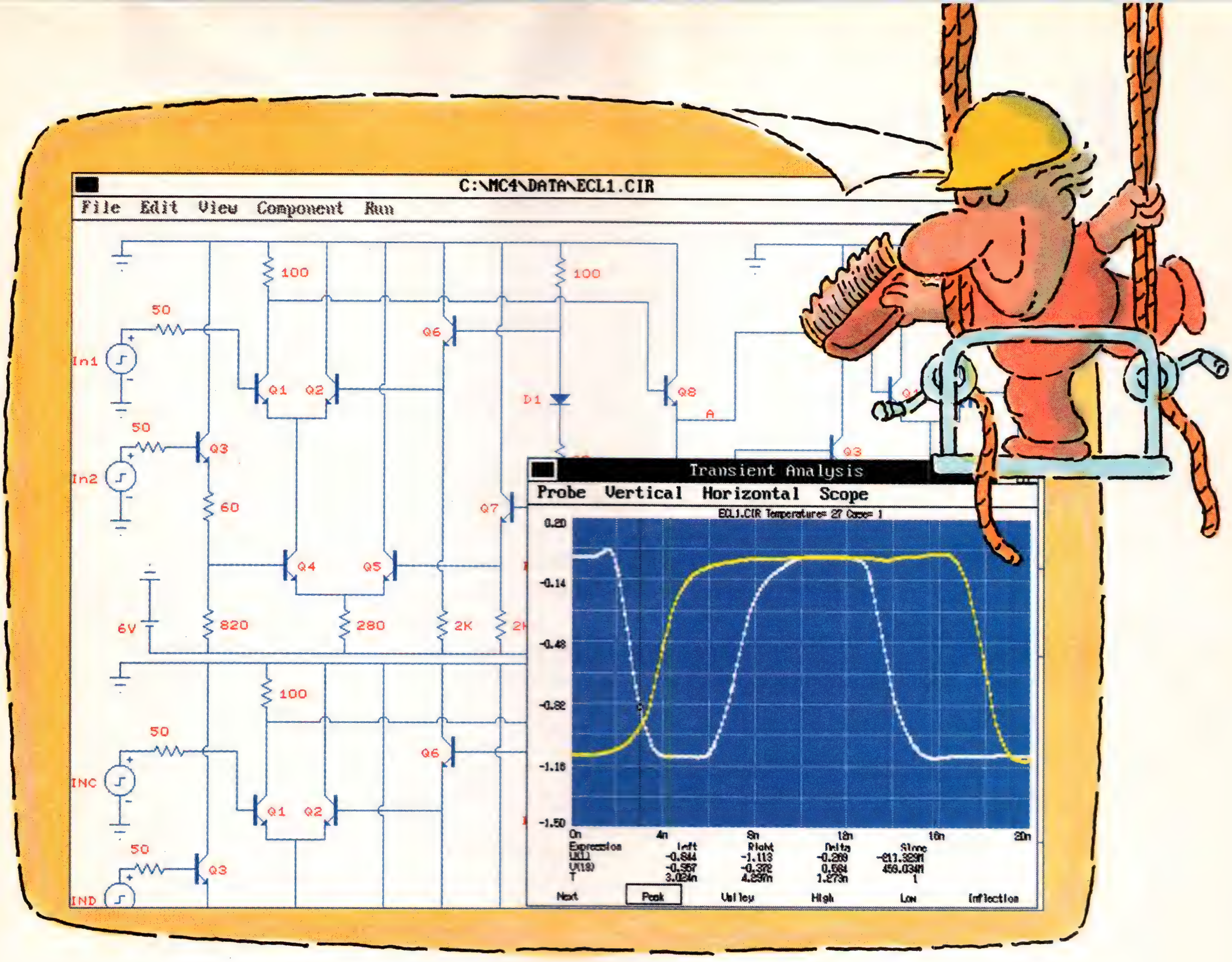
Fig 2—The power loss for Fig 1's current distribution is 345W—5.5 times the loss predicted by the conventional approach.

Good things come in small packages

The temperature in the office was becoming unbearable and my E-mail box was full of complaints about the heat. I needed to see how the temperature fluctuated during the day and then find the problem. Hooking up a data-acquisition board and temperature sensor to a PC, and then getting software to record the temperatures seemed like a lot of effort. Dan Strassberg loaned me a miniature stand-alone temperature data logger. The device—called Hobo-Temp—comes on a 4×3-cm circuit board, which includes the temperature sensor, a battery, and a connector. The connector links the Hobo-Temp to a PC or Apple Macintosh through the computer's serial port. After you download your instructions, or upload data, you snap a lid on the plastic bottle that contains the unit, and it operates on its own.

The accompanying software includes programs that run on a Macintosh computer or on a PC under DOS or Windows. I chose the DOS version of the software and quickly printed the standard README documentation from the disk. The DOS software runs from the DOS command line. You type in the name of the control program followed by the commands and switches that operate the temperature logger. The software gives you many choices. Programs check the data logger and the serial port you're using; run the logger and acquire the data; store it on disk; and convert the data file to one of several formats.

For example, you can set up the Hobo-Temp to acquire data using 31 intervals from 0.5 seconds to 4.8 hours, or for durations of 15 minutes to 360 days, respectively. The unit acquires and stores 1800 measurements. Each sample also has a



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Expression      Left      Right     Delta     Slope
V(1)          -0.844    -1.113    -0.269  -811.329M
V(18)         -0.567    -0.372     0.584   459.034M
T              3.024n    4.297n    1.273n   1
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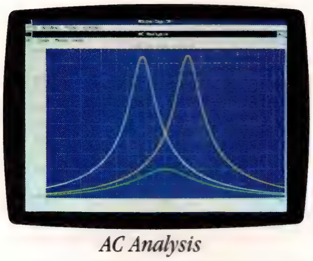

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"time stamp," so you know when it was taken. A ½AA-size battery powers the unit as it acquires data, and it maintains the measurements in memory until you transfer them to your computer.

As you program the unit for a data-acquisition period, you can also set other operation modes, for example, how the unit reports temperature. After programming is complete—it takes place as quickly as you can type in the options you need—you disconnect the device from your computer, and it takes temperature readings. My unit could measure temperature between −39 and +123°C, and it has a resolution of 0.6°C. You can also purchase units with a range of −5 to +37°C, or −37 to +46°C. The unit with the widest temperature range is accurate to within 1.7°C. (The accuracy and resolution figures become smaller as the range decreases.) The cost of individual units is $99. A complete starter kit, which includes cables and software, costs $149.

I acquired temperature data for most of the working day, dropped the unit in my briefcase, and took it home. Transferring data from the logger to my computer required another series of simple commands. I saved the data in comma-delimited format, so it was fairly easy to get it into a spreadsheet program (Quattro) and then plot it using PS-Plot.

Was it hot? You bet. The temperature went from just over 76°F (24.4°C) in the morning to 80°F (26.6°C) when I left the office. Now that the building maintenance man has sole control of the thermostat, it's a comfortable 70°F (21°C) all day. My next project involves measuring the temperatures in my favorite bass-fishing holes when the weather warms up. The Hobo-Temp has more practical uses, so if you're involved in measuring environmental conditions, it deserves a close look. It helped me solve a real problem.—**Jon Titus**

Onset Computer Corp, 199 Main St, Box 1030, North Falmouth, MA 02556. Phone (508) 563-9000. FAX (508) 653-9477.

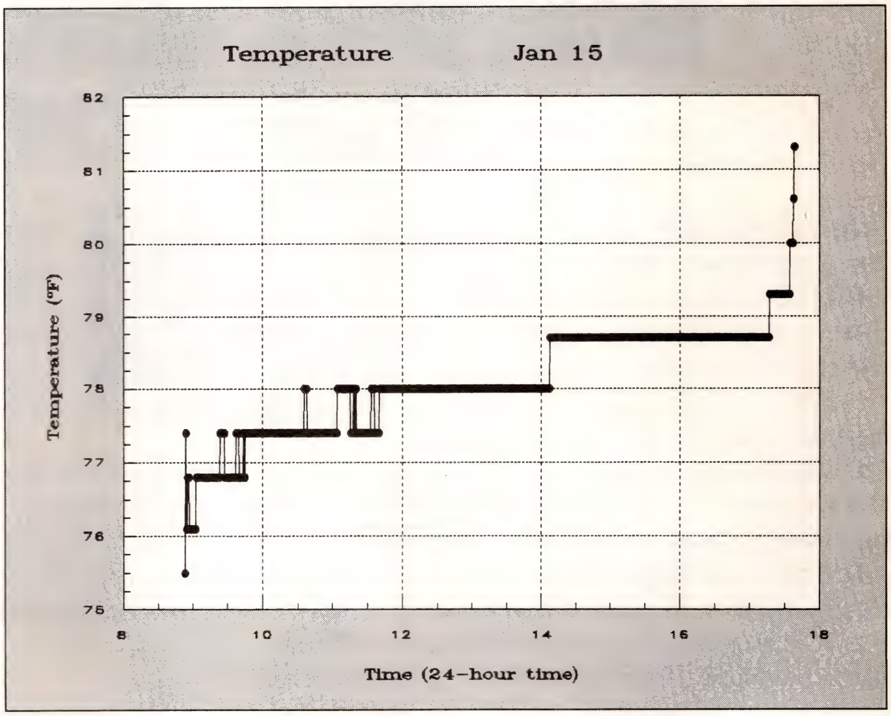
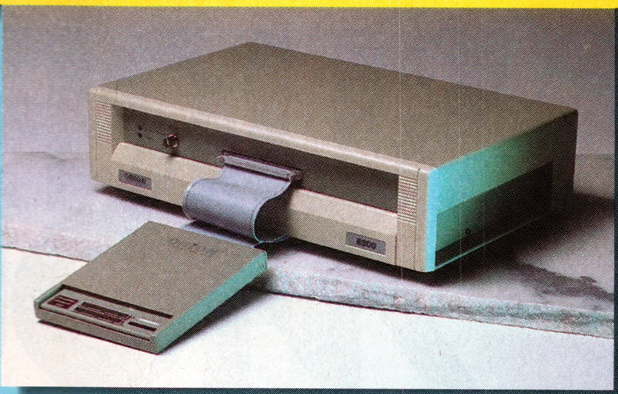


Fig 1—Hobo-Temp measured temperatures from about 9 am to 5:30 pm. The graph shows how the temperature rose during working hours.

EDN·ACRONYMS & ABBREVIATIONS

ACL—advanced CMOS logic
ADC—analog-to-digital converter
BiCMOS—bipolar CMOS
BIOS—basic I/O system
BNC—baby Neill Concelman (connector)
BW—bandwidth
CAE—computer-aided engineering
CMOS—complementary metal-oxide semiconductor
CPU—central processing unit
dB—decibel
DDE—Windows dynamic data-exchange protocol
DIP—dual in-line package
DLL—Windows dynamic link library
DRAM—dynamic random-access memory
DUT—device under test
DVM—digital voltmeter
EEPROM—electrically erasable programmable read-only memory
EGA—enhanced graphics adapter
EPROM—erasable programmable read-only memory
f—frequency
FPGA—field-programmable gate array
FPS—front-panel setting
I/O—input/output
IC—integrated circuit
LED—light-emitting diode
OTP—one-time-programmable (memory)
PC—personal computer
PCMCIA—Personal Computer Memory Card International Association
PLCC—plastic leaded chip carrier
PLD—programmable logic device
QSOP—quad small-outline package
RAM—random-access memory
ROM—read-only memory
SMA—push-on connector type
SMB—connector type
SOIC—small-outline integrated circuit
SPI—serial peripheral interface
TSSOP—thin shrink small-outline package
TTL—transistor-transistor logic
UART—universal asynchronous receiver transmitter
VGA—video graphics adapter
XIP—execute in place

80C196 68302 68EC000 68HC11(5+ MHz) Z180(20 MHz)



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Support today's fastest processors without wait-states—*at all times.*	Yes	☐
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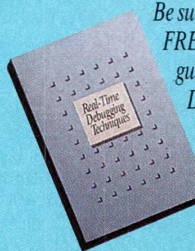

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80C186, 68332, 68HC16 available soon.

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IF	DC-500		DC-500		DC-500		DC-500	
Conversion Loss (dB)								
mid-band	6.0		6.0		5.5		5.7	
total range	6.5		7.0		5.5		6.4	
Isolation (dB)	(L-R)	(L-I)	(L-R)	(L-I)	(L-R)	(L-I)	(L-R)	(L-I)
low-band	60	50	50	55	28	18	35	18
mid-band	45	45	40	40	28	18	35	18
high-band	40	40	35	30	28	18	35	18
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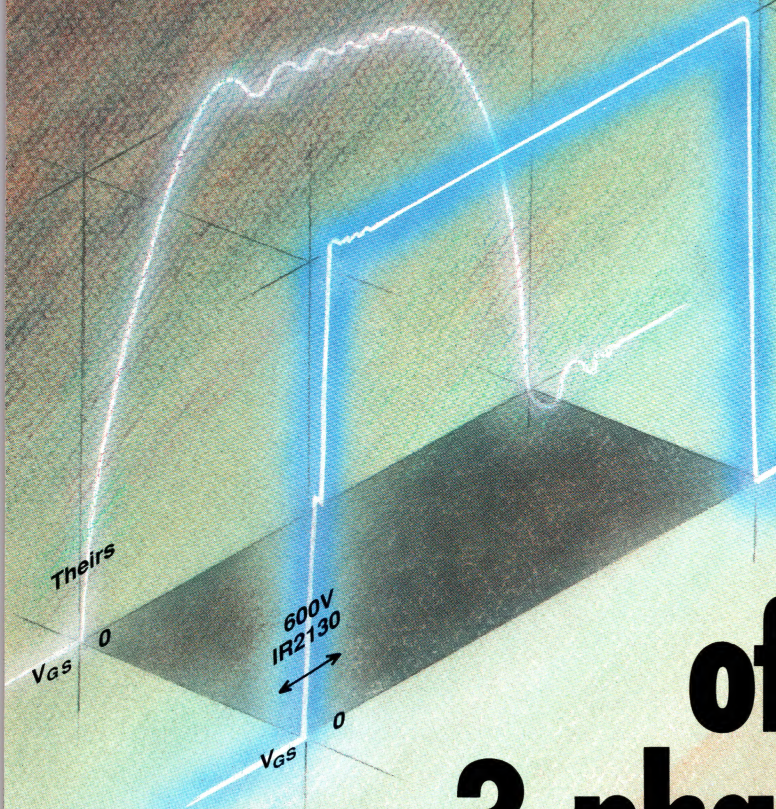

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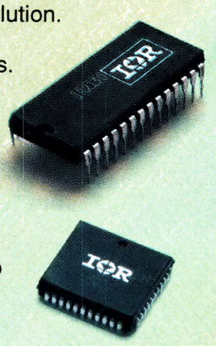

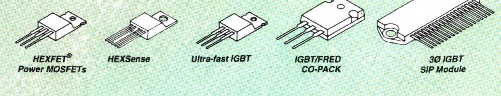

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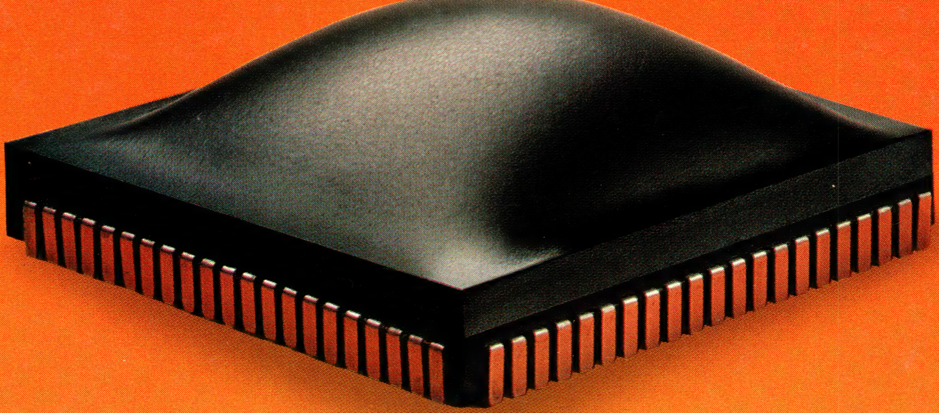

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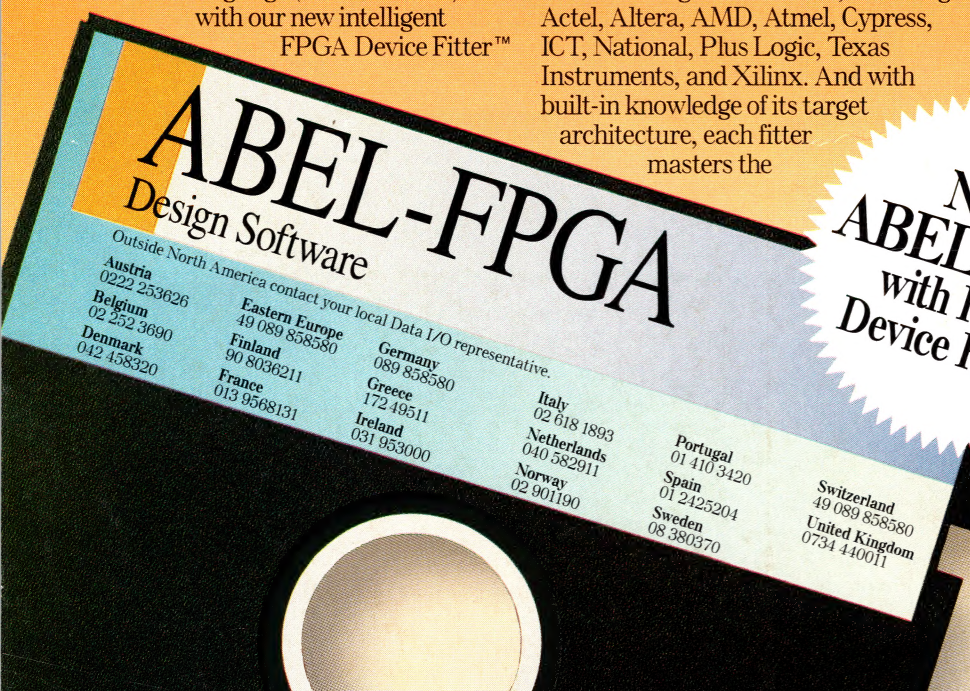

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